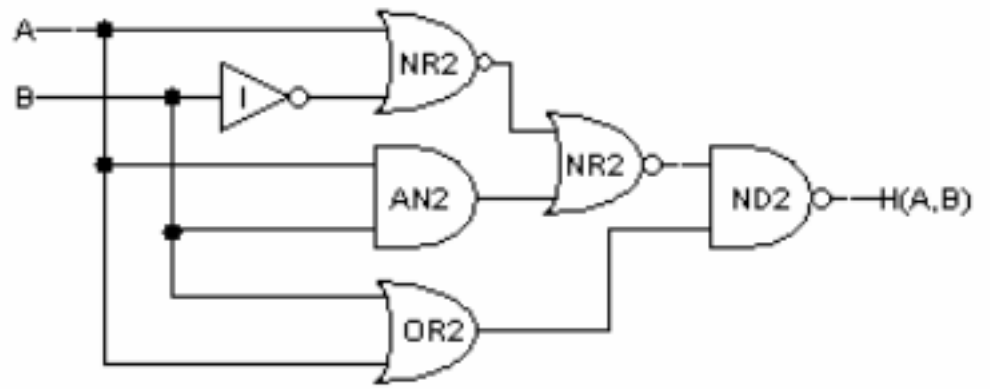
6.004 Computation Structures
Spring 2009

Gates and Boolean logic

Problem 1. Consider the following circuit that implements the 2-input function H(A,B):



A. ★ Fill in the following truth table for H:

A	B	H
0	0	
0	1	
1	0	
1	1	

B. ★ Give a sum-of-products expression that corresponds to the truth table above.

C. ★ Using the following table of timing specifications for each component, what are t_{CD}, t_{PD} and t_R for the circuit shown above?

gate	t_{CD}	t_{PD}	t_R	t_F
I	3ps	15ps	8ps	5ps
ND2	5ps	30ps	11ps	7ps
AN2	12ps	50ps	13ps	9ps

NR2	5ps	30ps	7ps	11ps
OR2	12ps	50ps	9ps	13ps

Problem 2. **Gates and Boolean equations**

A. Show the Boolean equation for the function F described by the following circuit:

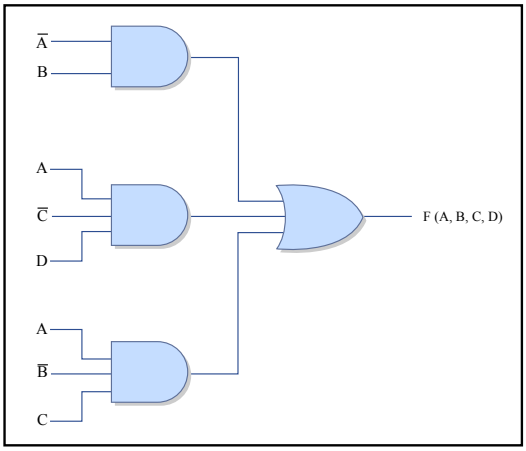


Figure by MIT OpenCourseWare.

B. ★ Consider the circuit shown below. Each of the control inputs, C0 through C3, must be tied to a constant, either 0 or 1.

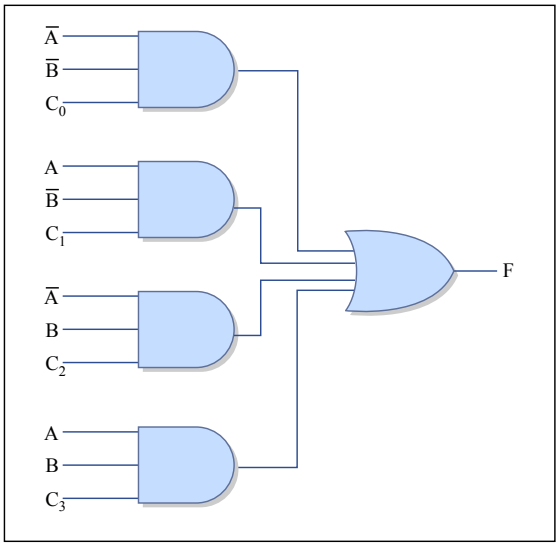


Figure by MIT OpenCourseWare.

What are the values of C0 through C3 that would cause F to be the *exclusive OR* of A and B?

C. ★ Can any arbitrary Boolean function of A and B be realized through appropriate wiring of the control signals C0 through C3?

D. Give a sum-of-products expression for each of the following circuits:

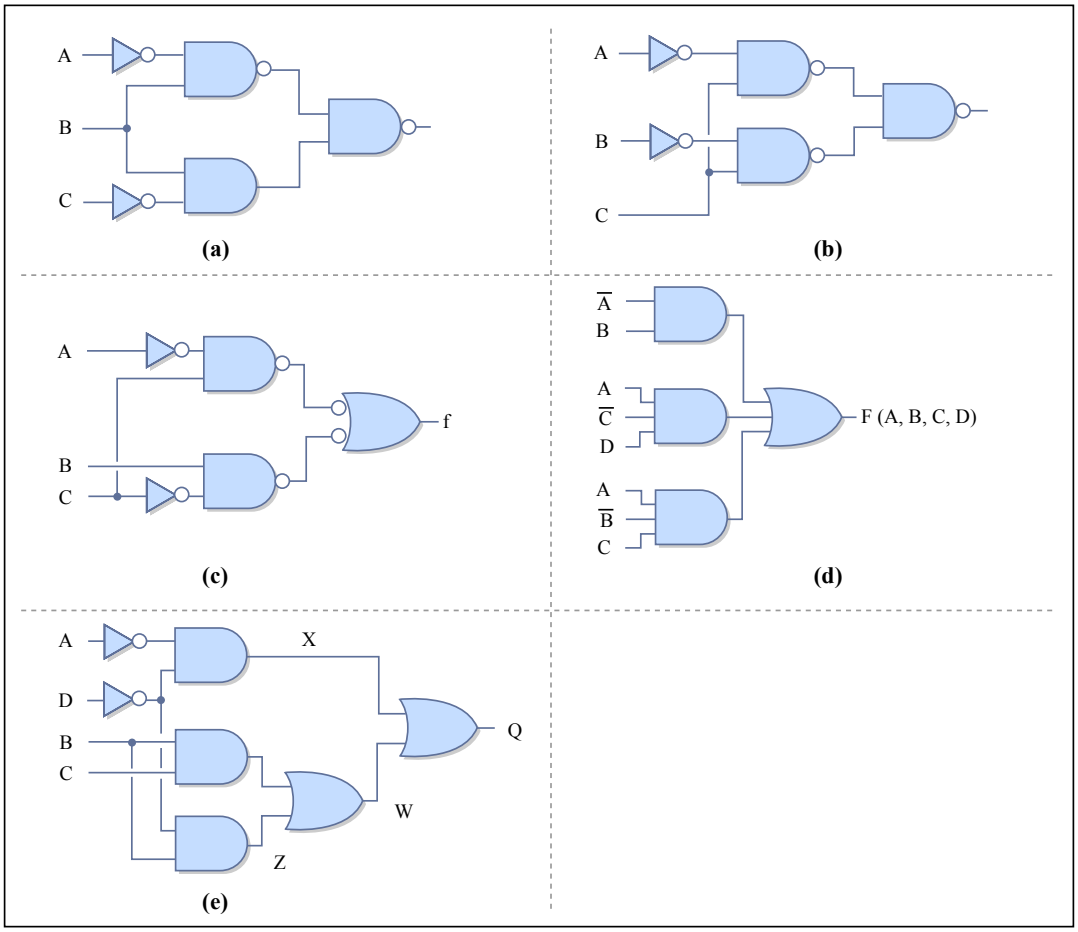


Figure by MIT OpenCourseWare.

E. Give a canonical sum-of-products expression for the Boolean function described by each truth table below

A	B	C	$F(A,B,C)$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

A	B	C	$G(A,B,C)$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

F. We've seen that there are a total of sixteen 2-input Boolean functions. How many 5-input Boolean functions are there?

Problem 3. A priority encoder has inputs that are assigned some predetermined order. The output is the binary encoding of the first "1" valued input from the ordered list, and it is zero otherwise.

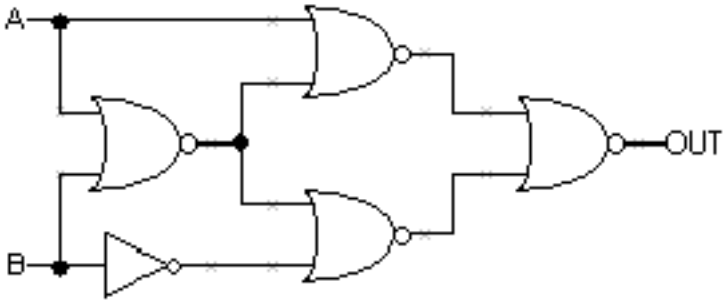
A. ★ Give the truth table for a 3-input priority encoder.

B. ★ Give a sum of products realization of this priority encoder.

Problem 4. Suppose we are building circuits using only the following three components:

- inverter: tcd = 0.5ns, tpd = 1.0ns, tr = tf = 0.7ns
- 2-input NAND: tcd = 0.5ns, tpd = 2.0ns, tr = tf = 1.2ns
- 2-input NOR: tcd = 0.5ns, tpd = 2.0ns, tr = tf = 1.2ns

Consider the following circuit constructed from an inverter and four 2-input NOR gates:



A. ★ What is t_{PD} for this circuit?

B. ★ What is t_{CD} for this circuit?

C. ★ What is the output rise time for this circuit?

D. ★ What is t_{PD} of the *fastest* equivalent circuit (i.e., one that implements the same function) built using only the three components listed above?

Problem 5. Suppose that each component in the circuit below has a propagation delay (tpd) of 10ns, a contamination delay (tcd) of 1ns, and negligable rise and fall times. Suppose initially that all four inputs are 1 for a long time and then the input D changes to 0.

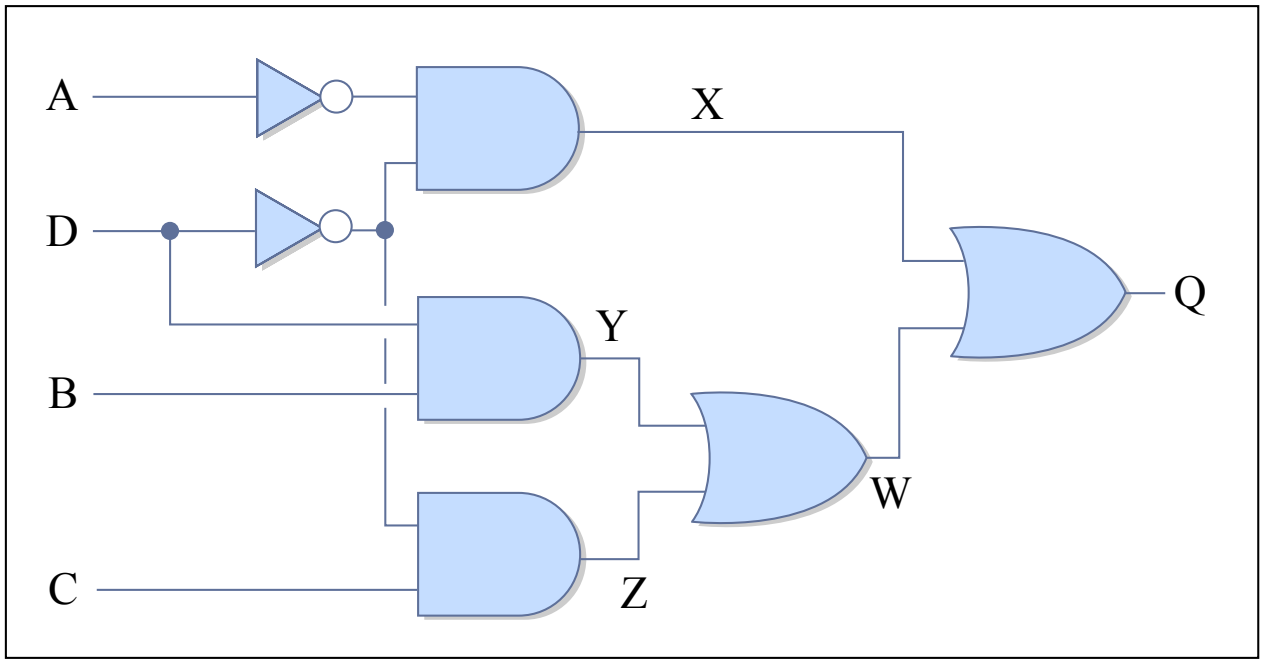
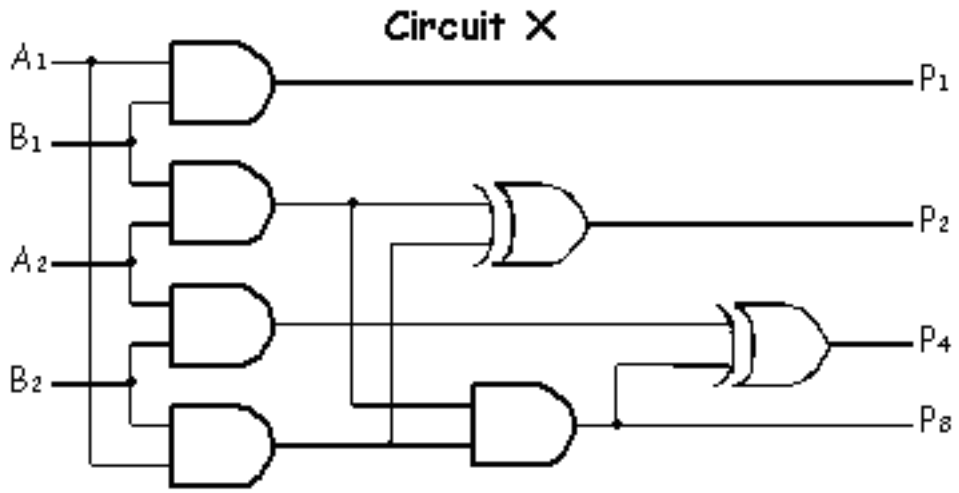


Figure by MIT OpenCourseWare.

A. Draw a waveform plot showing how X, Y, Z, W and Q change with time after the input transition on D. First assume that the gates are *not* lenient. How will the waveforms change if the gates are lenient?

Problem 6. **The Mysterious Circuit X**

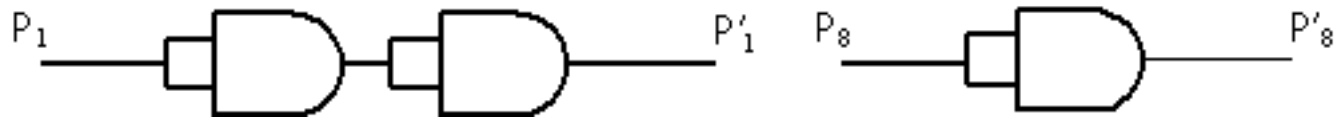
A. Determine the function of the Circuit X, below, by writing out and examining its truth table. Give a minimal sum-of-products Boolean expression for each output.



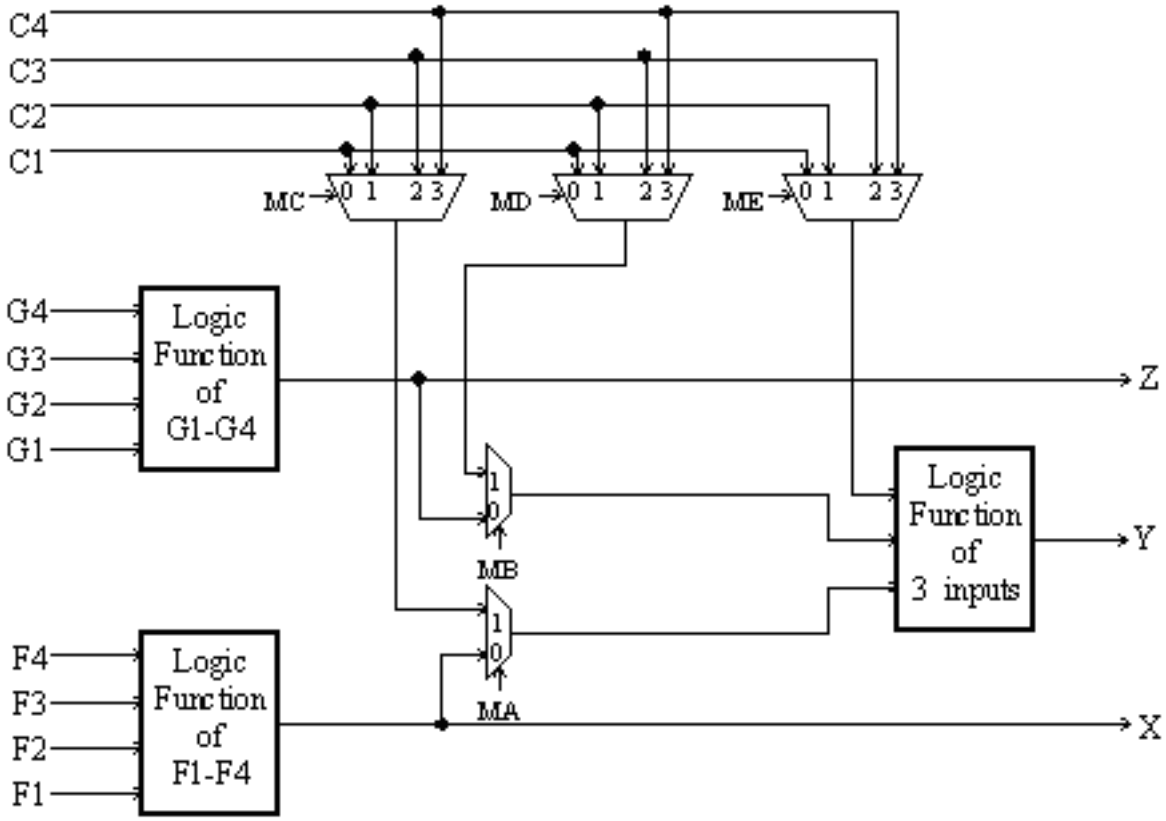
B. For Circuit X assume that AND gates have a propagation of 2 nS and a contamination delay of 1nS, while XOR gates have a propagation delay of 3 nS and contamination delay of 2 nS.

   Compute the aggregate contamination and propagation delays for Circuit X. What is the maximum frequency that the inputs of Circuit X be changed while insuring that all outputs are stable for 5 nS?

C. Suppose the gates below are added to Circuit X. How are the answers to part b) affected?



Problem 7. The Xilinx 4000 series field-programmable gate array (FPGA) can be programmed to emulate a circuit made up of many thousands of gates; for example, the XC4025E can emulate circuits with up to 25,000 gates. The heart of the FPGA architecture is a configurable logic block (CLB) which has a combinational logic subsection with the following circuit diagram:



There are two 4-input function generators and one 3-input function generator, each capable of implementing an arbitrary Boolean function of its inputs.

The function generators are actually small 16-by-1 and 8-by-1 memories that are used as lookup tables; when the Xilinx device is "programmed" these memories are filled with the appropriate values so that each generator produces the desired outputs. The multiplexer select signals (labeled "Mx" in the diagram) are also set by the programming process to configure the CLB. After programming, these Mx signals remain constant during CLB operation.

The following is a list of the possible configurations. For each configuration indicate how each the control signals should be programmed, which of the input lines (C1-C4, F1-F4, and G1-G4) are used, and what output lines (X, Y, or Z) the result(s) appear on.

A. An arbitrary function F of up to four input variables, plus another arbitrary function G of up to four unrelated input variables, plus a third arbitrary function H of up to three unrelated input variables.

B. An arbitrary single function of five variables.

C. An arbitrary function of four variables together with some functions of six variables. Characterize the functions of six variables that can be implemented.

D. Some functions of up to nine variables. Characterize the functions of up to nine variables that can

be implemented.

E. [Optional challenge] Can every function of six inputs be implemented? If so, explain how. If not, give a 6-input function and explain why it can't be implemented in the CLB.