May 24, 2001 - Final Exam

Name: SOLUTIONS

Recitation: _____

problem	grade
1	
2	
3	
4	
5	
total	

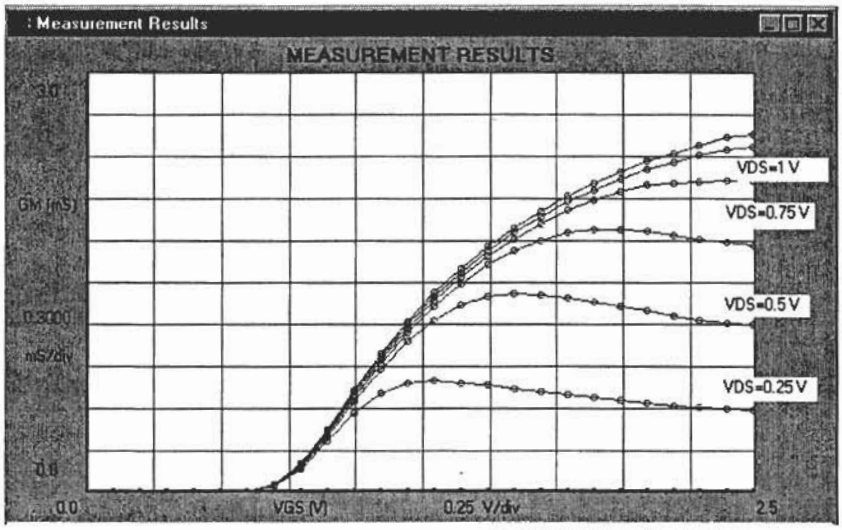
General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have **180 minutes** to complete your exam.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$n_i = 1 \times 10^{10}\ cm^{-3}$
$kT/q = 0.025\ V$
$q = 1.60 \times 10^{-19}\ C$
$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$
$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$

1. *(15 points)* The figure below shows the measured transconductance characteristics of the n-channel MOSFET that you characterized in *Device Characterization Project #2.* Each of the lines represents a different value of V_{DS}, starting with $V_{DS,min} = 0.25\ V$, in steps of $\Delta V_{DS} = 0.25\ V$.

This device has $L = 1.5\ \mu m$ and $W = 46.5\ \mu m$.



(1a) *(10 points)* In the space below, carefully sketch the g_m vs. V_{GS} characteristics predicted by the *ideal* MOSFET model presented in 6.012. Indicate the evolution of g_m for several values of V_{DS}. Derive suitable equations for each of the branches that you identify.

For V_{GS} right above threshold, the MOSFET is in saturation. g_m is given by:

$$g_m = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T)$$

which is linearly dependent on V_{GS} and independent of V_{DS}.

As V_{GS} increases, the device eventually goes into the linear regime. In this regime:

$$g_m = \frac{W}{L} \mu_n C_{ox} V_{DS}$$

which is linearly dependent on V_{DS} but independent of V_{GS}.

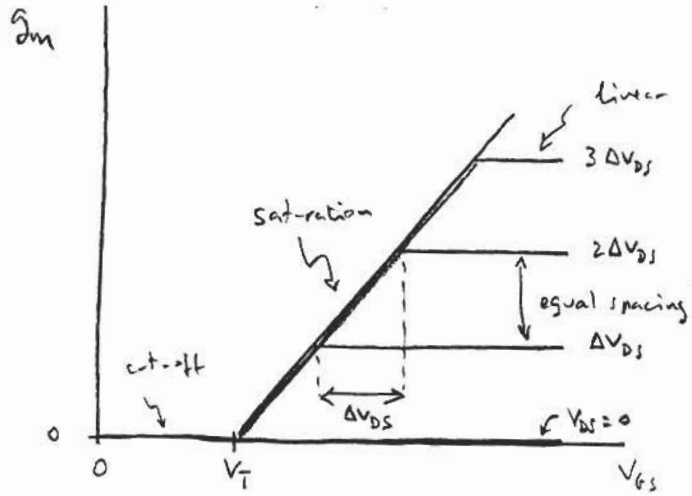
The boundary between the linear and saturation regimes is given by:

$$V_{DS} = V_{GS} - V_T$$

or

$$V_{GS} = V_{DS} + V_T$$

Assembling everything, the g_m characteristics of an ideal MOSFET ought to look like:



(1b) *(5 points)* From the data shown in the figure above, estimate V_T and $\mu_n C_{ox}$ for the measured device.

V_T can be estimated from the onset of g_m:

$$V_T \simeq 0.7 \text{ V}$$

We can get an estimate for the value of $\mu_n C_{ox}$ by evaluating the transconductance for the first line, the one that corresponds to $V_{DS} = 0.25$ V. From

$$g_m = \frac{W}{L} \mu_n C_{ox} V_{DS}$$

we solve for $\mu_n C_{ox}$:

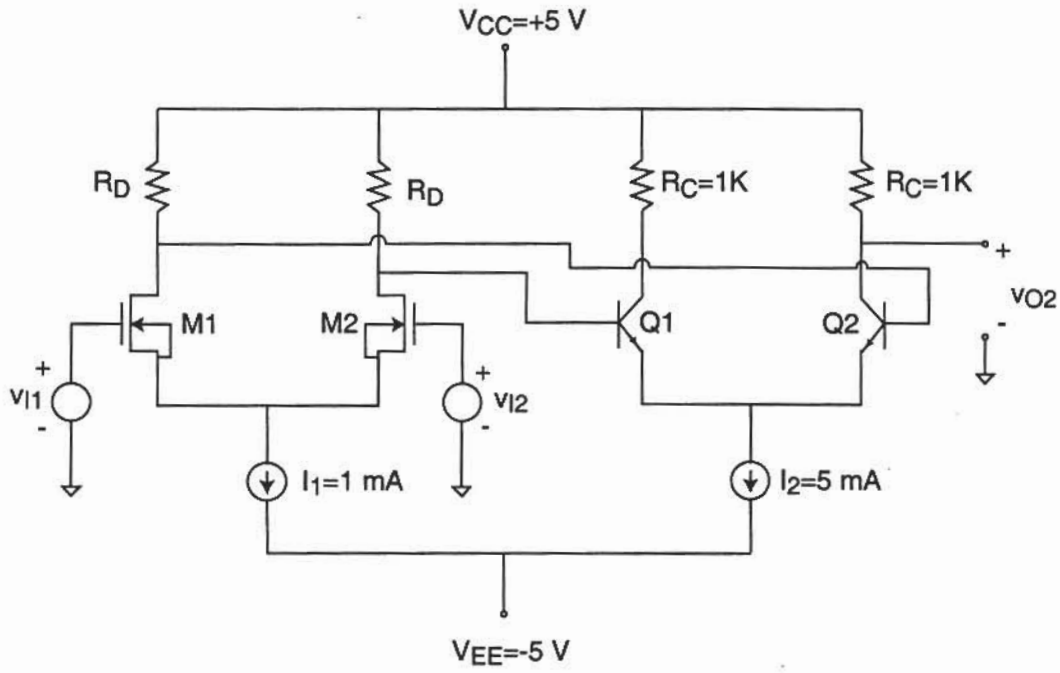
$$\mu_n C_{ox} = \frac{g_m L}{W V_{DS}}$$

An average value of g_m in this branch is ~ 0.7 mS. Then

$$\mu_n C_{ox} = \frac{0.7 \times 10^{-3} \times 1.5}{46.5 \times 0.25} = 9 \times 10^{-5} \text{ A/V}^2 = 90 \ \mu\text{A/V}^2$$

which is reasonable.

2. *(15 points)* Consider the two-stage BiCMOS differential amplifier below.



M1 and M2 are identical and are biased in the saturation regime. Q1 and Q2 are also identical and are biased in the forward active regime. Suitable parameters for these transistors are:

nMOSFET: $V_T = 1\ V$ and $\frac{W}{L}\mu_n C_{ox} = 0.1\ mA/V^2$

npn BJT: $\beta_F = 250$, $V_{BEon} = 0.7\ V$ and $V_{CEsat} = 0.2\ V$

The current sources I_1 and I_2 need at least $0.5\ V$ across to operate properly.

(2a) *(5 points)* Compute the power dissipation of this amplifier.

The total current flowing from V_{CC} to V_{EE} is $I_1 + I_2 = 6\ mA$.

The power dissipated is then:

$$W = (V_{CC} - V_{EE})(I_1 + I_2) = 10\ V \times 6\ mA = 60\ mW$$

(2b) *(5 points)* What constraint is imposed on R_D so that the amplifier can properly handle a *maximum common-mode input* of 3 V? (Express your answer as $R_D > X$ *or* $R_D < X$. Give value of X).

With a common-mode input, the drains of M1 and M2 are fixed at

$$V_D = V_{CC} - \frac{I_1}{2} R_D$$

For M1 and M2 to remain in saturation, V_D has to be above the gate voltage of these transistors minus the threshold voltage. That is,

$$V_D > V_{icmax} - V_T$$

Then we need:

$$V_{CC} - \frac{I_1}{2} R_D > V_{icmax} - V_T$$

or

$$R_D < \frac{2}{I_1} (V_{CC} + V_T - V_{icmax}) = \frac{2}{1mA} (5 + 1 - 3) = 6\ k\Omega$$

(2c) *(5 points)* If $R_D = 5\ k\Omega$, what is the maximum possible voltage swing of node V_{O2} with respect to ground? Give V_{O2min} and V_{O2max}.

V_{O2min} could be set in two ways. First it could be set when all the current of the second differential pair swings over to Q2. In this case:

$$V_{O2min} = V_{CC} - I_C R_C = 5 - 5\,mA \times 1\,k\Omega = 0\ V$$

But it could also be set by Q2 being driven into saturation. For $R_D = 5\ k\Omega$, the base of Q2 is at

$$V_B = V_{CC} - R_D \frac{I_1}{2} = 5 - 5\,k\Omega \times 0.5\,mA = 2.5\ V$$

Then when Q2 goes into saturation

$$V_{O2min} = V_B - V_{BEon} + V_{CEsat} = 2.5 - 0.7 + 0.2 = 2.0\ V$$

Since this is higher than V_{O2min} calculated above, this is the most restrictive. Hence

$$\boxed{V_{O2min} = 2.0\ V.}$$

V_{O2max} could occur when all the current swings over to Q1. This would give $V_{O2max} = 5\ V$. But also when Q1 goes into saturation. We know this happens when $V_{C1} = 2\ V$. Then

$$I_{C1} = \frac{V_{CC} - V_{C1}}{R_C} = \frac{5 - 2.0}{1\,k} = 3\ mA$$

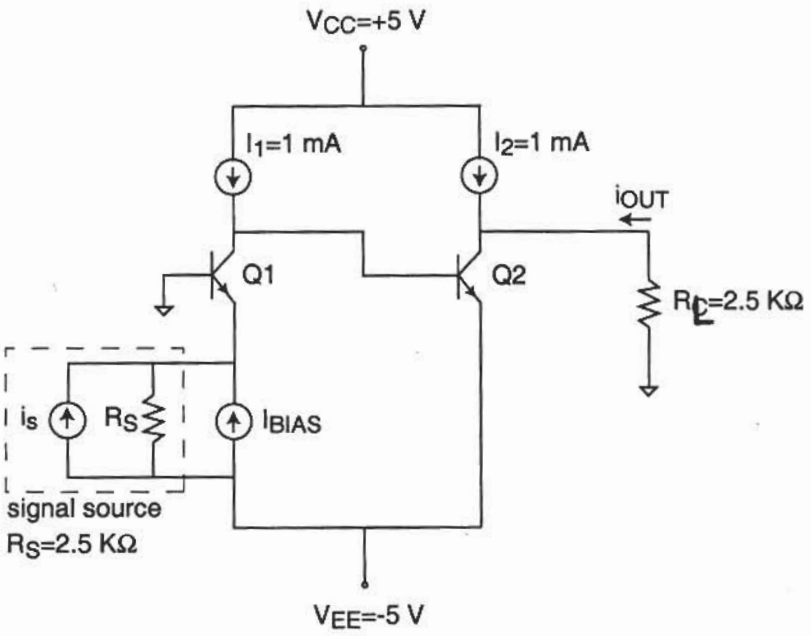
Hence $I_{C2} = 2\ mA$, and

$$\boxed{V_{O2\,max} = V_{CC} - I_{C2} \times R_C = 5 - 2 \times 1 = 3\ V}$$

This is more restrictive. The total voltage swing is

$$\boxed{V_{OUTswing} = 1\ V}$$

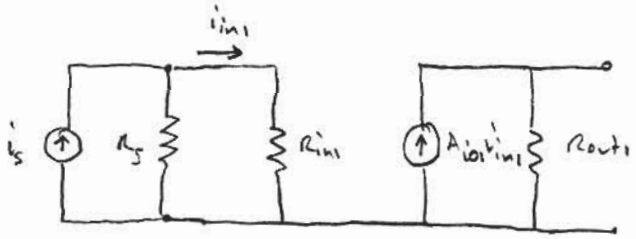
3. *(25 points)* Consider the two-stage bipolar current amplifier shown below. At the input of this amplifier there is a signal source with an internal resistance $R_S = 2.5\ k\Omega$; at the output, there is a load characterized by $R_L = 2.5\ k\Omega$.



Both transistors in this amplifier are identical and are characterized by the following parameters: $\beta_F = 100$ and $V_A = 50\ V$. Treat all biasing current sources as ideal, that is, with infinite internal resistance.

(3a) *(10 points)* Draw a two-port low-frequency small-signal equivalent-circuit model of the first stage of this amplifier. Derive values for all elements of this two-port model.

A suitable equivalent circuit model for the first stage is:



Rin1, Rout1 and Aio are function of the small signal parameters of the bipolar transistor, which are:

$$g_{m1} = \frac{q\bar{I}_{C1}}{kT} = \frac{1\ mA}{0.026} = 40\ mS$$

$$r_{\pi 1} = \frac{\beta_F}{g_{m1}} = \frac{100}{40\ mS} = 2.5\ k\Omega$$

$$r_{o1} = \frac{V_A}{\bar{I}_C} = \frac{50\ V}{1\ mA} = 50\ k\Omega$$

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We now know from the notes that for the common-base stage:

$$R_{in1} = \frac{1}{g_{m1}} = 25\ \Omega$$

$$A_{i01} \simeq -1$$

$$R_{out1} = r_{o1}\left[1 + g_{m1}\left(r_{\pi1} \,//\, R_S\right)\right]$$

The parallel of $r_{\pi1}$ and R_S is:

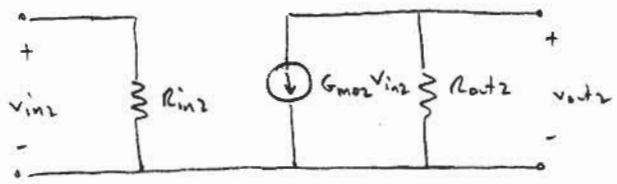
$$r_{\pi1} \,//\, R_S = \frac{1}{\frac{1}{r_{\pi1}} + \frac{1}{R_S}} = \frac{1}{\frac{1}{2.5} + \frac{1}{2.5}} = 1.25\ k\Omega$$

Then

$$R_{out} = 50k\ (1 + 40 \times 1.25) = 2.6\ M\Omega$$

(3b) *(10 points)* Draw a two-port low-frequency small-signal equivalent-circuit model of the second stage of this amplifier. Derive values for all elements of this two-port model.

The second stage of this amplifier is a common-emitter stage. Hence, a suitable two-port description is



Since the current through the second transistor is also 1 mA, the small-signal parameters for Q2 have the same value as those of Q1. Then, from the notes:

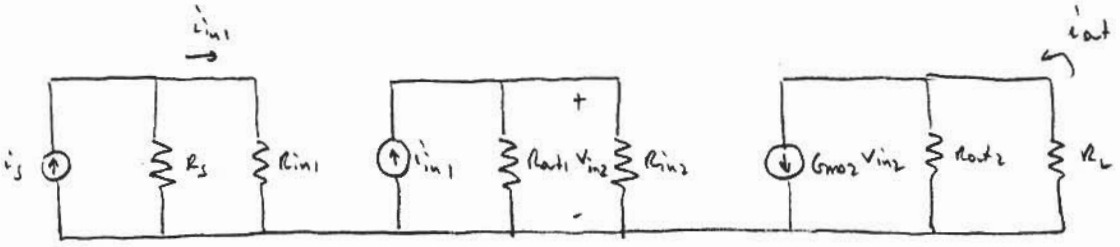
$$R_{in2} = r_{\pi 2} = 2.5\ k\Omega$$

$$G_{mo2} \simeq g_{m2} = 40\ mS$$

$$R_{out2} = r_{o2} = 50\ k\Omega$$

(3c) *(5 points)* Calculate the *loaded current gain* $A_i = \frac{i_{out}}{i_s}$ of this amplifier.

Assembling the whole thing now:



At the input of the first stage, $R_s \gg R_{in1}$, hence

$$i_{in1} \simeq i_s$$

Between the two stages, $R_{out1} \gg r_{in2}$, hence

$$v_{in2} \simeq i_{in1} R_{in2}$$

At the output of the second stage, $R_{out2} \gg R_L$, then

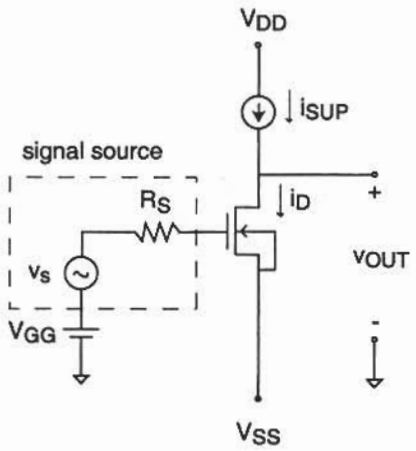
$$i_{out} \simeq G_{mo2} v_{in2}$$

Assembling everything

$$A_i = \frac{i_{out}}{i_s} = \frac{i_{out}}{v_{in2}} \times \frac{v_{in2}}{i_{in1}} \times \frac{i_{in1}}{i_s} = G_{mo2} R_{in2} =$$

$$= 40\,mS \times 2.5\,k\Omega = 100$$

4. *(15 points)* The diagram below shows an *unloaded* common-source amplifier with a current source supply. The adjoining table describes the relationship between device parameters and circuit parameters for this amplifier stage.



Device * Parameters	Circuit Parameters			
	$\lvert A_{vo}\rvert$	R_{in}	R_{out}	ω_H
$I_{SUP}\uparrow$	$\downarrow$	-	$\downarrow$	$\uparrow$
$W\uparrow$	$\uparrow$	-	-	$\downarrow$
$\mu_n C_{ox}\uparrow$	$\uparrow$	-	-	$\downarrow$
$L\uparrow$	$\uparrow$	-	$\uparrow$	$\downarrow$

In this table, when changing one of the device parameters, adjustments are made to V_{GG}, the gate bias, so that none of the other parameters are affected.

In this problem, you have to fill the fourth column of this table that contains the 3dB bandwidth of the amplifier. Use the same format as in the rest of the table and indicate in what direction ω_H will change when the device parameters increase one at a time. Nothing else changes, except perhaps for V_{GG} as explained above. In the space below, provide an explanation for your entry. *If there is no explanation, there are no points!*

(4a) *(3 points)* If $I_{SUP}\uparrow$, how does ω_H change? Select: (↑) −, ↓. Why?

The 3dB bandwidth of a common-source stage is given by:

$$\omega_{3dB} \approx \frac{1}{R_S\left[C_{gs} + C_{gd}(1+|A_{v,LF}|)\right] + (r_o \| r_{oc})\, C_{db}}$$

If $I_{SUP}\uparrow$, as the table above indicates, $|A_{vo}|\downarrow$ and $R_{out} = r_o \| r_{oc}\downarrow$. Both things imply that $\omega_{3dB}\uparrow$.

(4b) *(3 points)* If $W \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, (↓) Why?

If $W\uparrow$ keeping the current constant, all capacitors increase in size and $|A_{vo}| \uparrow$. Then, all this implies in the formula that $\omega_{3dB} \downarrow$

(4c) *(3 points)* If $\mu_n C_{ox} \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, (↓) Why?

If $\mu_n C_{ox} \uparrow$ while keeping the current constant means that $|A_{vo}| \uparrow$. Then $\omega_{3dB} \downarrow$.

(4d) *(3 points)* If $L \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, (↓) Why?

If $L\uparrow$ while keeping the current constant, C_{gs} increases, also $|A_{vo}| \uparrow$ and $R_{out} = r_o \| r_{oc} \uparrow$, then $\omega_{3dB} \downarrow$

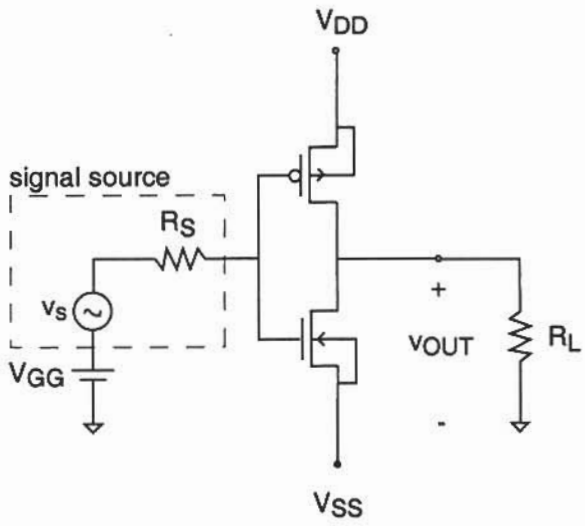
(4e) *(3 points)* If we now connect the output of the amplifier to a load resistance $R_L \ll r_o // r_{oc}$, how does ω_H change? Select: (↑) $-$, ↓. Why?

Connecting at the output $R_L << r_o \| r_{oc}$ means that

$$R_{out} = R_L \| r_o \| r_{oc} \approx R_L << r_o \| r_{oc}$$

Hence the time constant associated with C_{db} goes down and so does $|A_{v,LF}|$ due to the output loading. All this means that $\omega_{3dB} \uparrow$

5. *(30 points)* Consider the following CMOS amplifier:



The devices are characterized by the following parameters:

nMOS: $L_n = 1\ \mu m$, $W_n = 4\ \mu m$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{Tn} = 1\ V$, $\lambda_n = 0.1\ V^{-1}$, $C_{gsn} = 6\ fF$, $C_{gdn} = 1\ fF$, $C_{dbn} = 5\ fF$.

pMOS: $L_p = 1\ \mu m$, $W_p = 8\ \mu m$, $\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{Tp} = -1\ V$, $\lambda_p = 0.1\ V^{-1}$, $C_{gsp} = 12\ fF$, $C_{gdp} = 2\ fF$, $C_{dbp} = 10\ fF$.

Other values are: $V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $R_S = 1\ k\Omega$, and $R_L = 1\ k\Omega$.

(5a) *(5 points)* Compute the value of V_{GG} required to obtain a quiescent output voltage $V_{OUT} = 0\ V$.

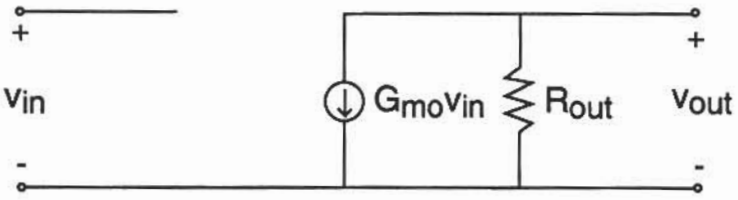
At low frequency, this is a completely symmetric inverter stage, since $V_{Tn} = -V_{Tp}$, $\frac{W_n}{L_n}\mu_n C_{ox} = \frac{W_p}{L_p}\mu_p C_{ox}$, and $\lambda_n = \lambda_p$. Then, in order to obtain a quiescent $V_{out} = 0$ V, we need $V_{GG} = 0$ V.

We could compute this also by noting that if $V_{out} = 0$, then there is no current through R_L and as a result; $I_{Dn} = I_{Dp}$. Then

$$I_D = \frac{1}{2}\frac{W_n}{L_n}\mu_n C_{ox}(V_{GG} - V_{SS} - V_{Tn})^2 = \frac{1}{2}\frac{W_p}{L_p}\mu_p C_{ox}(V_{DD} - V_{GG} + V_{Tp})^2$$

Solving this yields $V_{GG} = 0$ V.

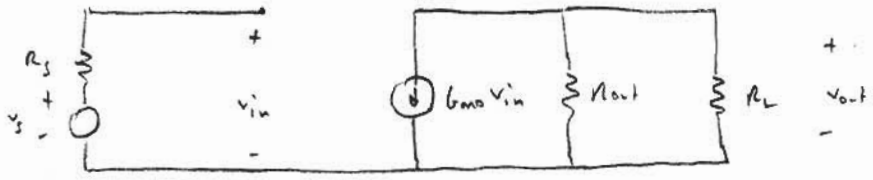
A low-frequency small-signal equivalent circuit model for this amplifier in an *unloaded* configuration at the bias point specified in part (5a) is given below:



with $G_{mo} = 1.6\ mS$ and $R_{out} = 3.1\ k\Omega$.

(5b) *(5 points)* Calculate the *loaded* voltage gain of the entire CMOS amplifier (don't be alarmed if it comes out a bit small, this is not a very good amplifier).

The complete small-signal equivalent circuit model for the entire amplifier is, then:



v_{out} is

$$v_{out} = -G_{mo}\,(R_{out} \,//\, R_L)\,v_{in}$$

and

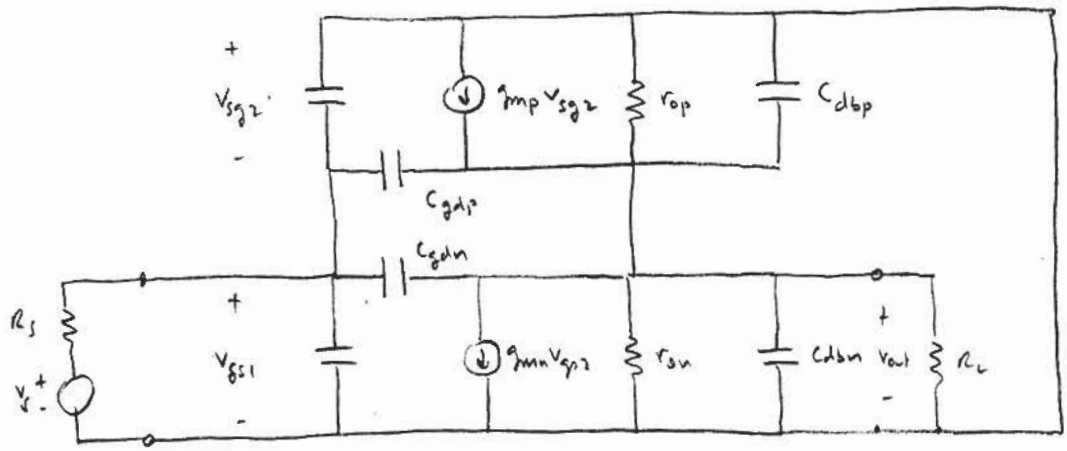
$$v_{in} = v_s$$

Then, the overall voltage gain is:

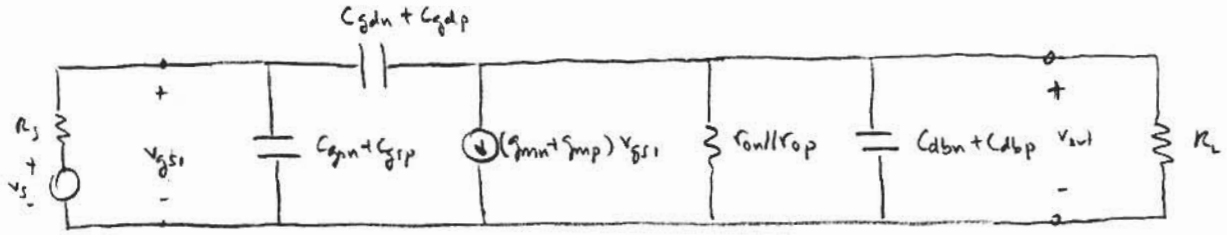
$$A_v = \frac{v_{out}}{v_s} = -G_{mo}\,(R_{out} \,//\, R_L) = -1.6\,\frac{1}{\frac{1}{3.1} + \frac{1}{1}} = -1.2$$

(5c) *(15 points)* Estimate the 3 dB bandwidth of the entire CMOS amplifier (that is, in its loaded configuration). To do this, calculate the time constant of each capacitor at a time *(six capacitors at 2 points each)*. Then compute the 3 dB bandwidth in *Hz (3 points)*.

A complete high-frequency small-signal equivalent circuit model of this stage is:



This can be collapsed in the following way:



It is easy to compute the time constants of each capacitor because the topology of this circuit is identical to that of a common-source stage.

C_{gsn} $\quad \tau_{gsn} = R_s C_{gsn} = 1k \times 6\times10^{-15}\,F = 6\times10^{-12}\,s$

C_{gsp} $\quad \tau_{gsp} = 2\tau_{gsn} = 12\times10^{-12}\,s$

C_{gdn} $\quad \tau_{gdn} \simeq R_s C_{gdn}(1+|A_{v1}|) = 1k \times 10^{-15}\,(1+1.2) = 2.2\times10^{-12}\,s$

C_{gdp} $\quad \tau_{gdp} = 2\tau_{gdp} \simeq 4.4\times10^{-12}\,s$

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R_{out}

C_{dbn} $\qquad \tau_{dbn} = C_{dbn} R_{out}' = C_{dbn} R_L // r_{on} // r_{op} =$

$$= 5\times10^{-15} \times \frac{1}{\frac{1}{1K} + \frac{1}{3.1K}} = 3.8\times10^{-12}\ s$$

C_{dbp} $\qquad \tau_{dbp} = 2\tau_{dbn} = 7.6\times10^{-12}\ s$

ω_H is then:

$$\omega_H = \frac{1}{\sum \tau_i} = \frac{1}{3\times 6\times10^{-12} + 3\times 2.2\times10^{-12} + 3\times 3.8\times10^{-12}} = 2.8\times10^{10}\ rad/s$$

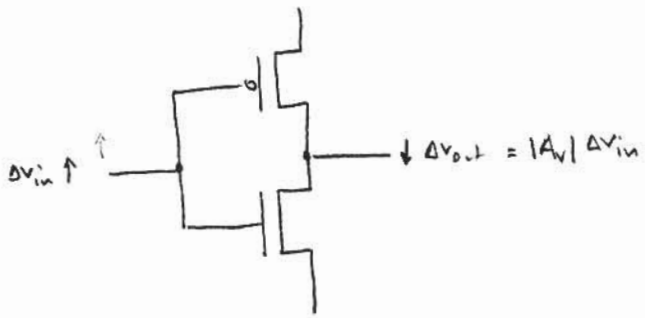
and in Hz

$$f_H = \frac{\omega_H}{2\pi} = 6.6\times10^{9}\ Hz = 4.4\ GHz$$

(5d) *(5 points)* Calculate the voltage swing of the output node of this amplifier in its loaded configuration.

The swing is limited by the PMOS going into the linear region. The downswing will be set by the NMOS going into the linear region. Since there is complete simmetry, the swing and the downswing are identical. We only need to compute one of them

We can easily compute the downswing in the following way.



The NMOS goes into the linear region when

$$V_{GD} = V_T$$

Since the quiescent bias for both the input and the output is 0, when V_+ swings up by ΔV_{in}, then

$$V_+ = \Delta V_{in}$$

$$V_D = -|A_v| \Delta V_{in}$$

Then $$V_{GD} = (1+|A_v|)\,\Delta V_{in} = V_T$$

So we have a problem when

$$\Delta V_{in} = \frac{V_T}{1+|A_v|} = \frac{1}{1+1.2} = 0.46\ V$$

The downswing at the output is

$$\Delta V_{out} = -|A_v| \Delta V_{in} = -1.2 \times 0.46 = -0.55\ V$$

And the total swing is then

$$V_{swing} = 2 \times 0.55 = 1.1\ V.$$

There are other ways to compute this

(5d) *(5 points)* Calculate the voltage swing of the output node of this amplifier in its loaded configuration.

The upswing is limited by the PMOS going into the linear region. The downswing will be set by the NMOS going into the linear region. Since there is complete symmetry, the upswing and the downswing are identical. We only need to compute one of them

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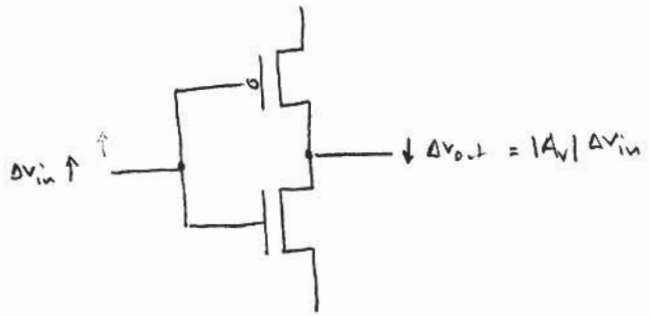

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$$\Delta V_{in} = \frac{V_T}{1+|A_v|} = \frac{1}{1+1.2} = 0.46\ V$$

The downswing at the output is

$$\Delta V_{out} = -|A_v| \Delta V_{in} = -1.2 \times 0.46 = -0.55\ V$$

And the total swing is then

$$V_{swing} = 2 \times 0.55 = 1.1\ V.$$

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