*YOUR NAME*________________________________

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

Final Exam

Wednesday, May 24, 2006
1:30 to 4:30 pm
Closed Book: Formula sheet provided; 3 sheets of notes permitted

Notes:

1. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate [(kT/q) ln 10] as 0.06 V.
2. Closed book; three sheets (6 pages) of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all thirteen (13) pages of this exam booklet and the six (6) page formula sheet, and make certain that you write your name at the top of this page in the space provided.
7. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.
8. You may see your graded final exam beginning June 1, 2006.

6.012 Staff Use Only			
	PROBLEM 1	__________	(out of a possible 25)
	PROBLEM 2	__________	(out of a possible 25)
	PROBLEM 3	__________	(out of a possible 25)
	PROBLEM 4	__________	(out of a possible 25)
	TOTAL		

Problem 1 - (25 points)

a) [4 pts] Consider a p^+-n junction diode with $N_{Ap} = 10^{18}$ cm^{-3} and $N_{Dn} = 10^{16}$ cm^{-3}, $\mu_e = 1500$ cm^2/V-s, $\mu_h = 500$ cm^2/V-s, and $W_p = W_n << L_{min}$. What is the largest component of the junction current with the following bias conditions? Explain.

i) Forward bias, $V_{AB} = 0.6$ V:

[ ] Holes / [ ] Electrons moving from the [ ] n-side to the p-side. / [ ] p-side to the n-side.

because

ii) Reverse bias, $V_{AB} = -2$ V

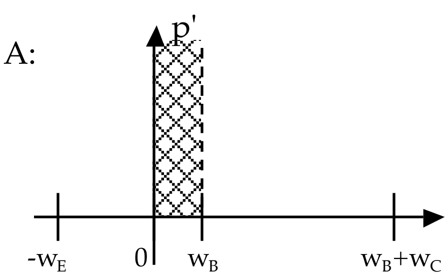
[ ] Holes / [ ] Electrons moving from the [ ] n-side to the p-side. / [ ] p-side to the n-side.

because

b) [6 pts] Consider a well designed npn bipolar junction transistor, with $N_{DE} = 4\,N_{AB} = 16\,N_{DC}$ and $W_C = 2W_E = 4W_B$, under two bias conditions: Condition A is $V_{BE} = 0.6$ V and $V_{BC} = 0$ V, and Condition B is $V_{BE} = 0$ V and $V_{BC} = 0.6$ V.

i) For which bias condition is the total number of injected excess minority carrier <u>holes</u> greatest? To explain why, sketch p' for each bias on the axes provided.

A:



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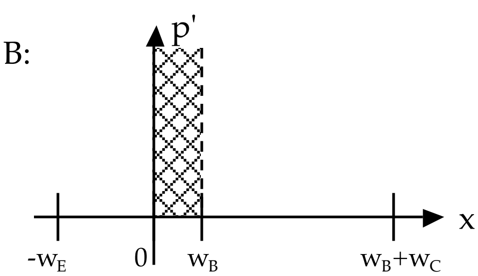
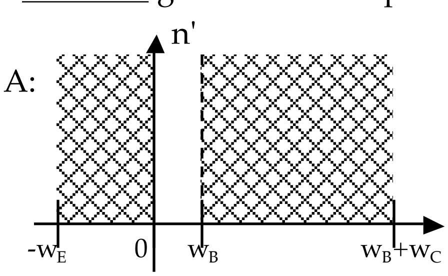


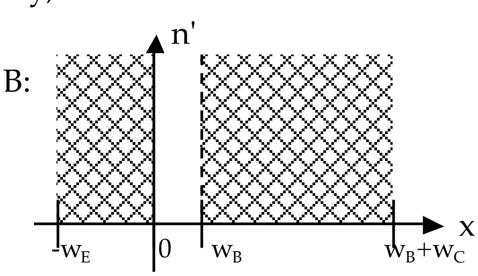
[ ] Bias Condition A [ ] Bias Condition B [ ] No difference

ii) For which bias condition is the total number of injected excess minority carrier <u>electrons</u> greatest? To explain why, sketch n' for each bias on the axes provided.

A:



B:



[ ] Bias Condition A [ ] Bias Condition B [ ] No difference

Problem 1 continues on the next page

Problem 1 continued

c) [6 pts] Suppose that a minimum size CMOS inverter has an input capacitance C_L, and can itself charge and discharge an identical linear capacitive load, C_L, in 10 ns.

i) How long does it take this same inverter to charge and discharge a linear capacitive load 36 C_L?

Time to charge and discharge 36 C_L: __________ ns

ii) Consider inserting a larger inverter between the minimum size inverter and the 36 C_L load in order to speed up the switching. What is the optimum size for this inverter, and how long does it take your choice to charge and discharge the 36 C_L load? Use only integer size multiples.

Optimum size (multiple of minimum width): _________________

Time to charge and discharge 36 C_L: __________ ns

d) [6 pts] Two emitter follower stages are used in otherwise identical multi-stage amplifiers in which they are biased in their forward active region with the same collector current. Stage A is made using a bipolar transistor with $\beta_F = 200$, and Stage B is made with a transistor for which $\beta_F = 50$.

i) Which emitter follower stage has the larger <u>input resistance</u>, and why?

[ ] Stage A larger [ ] Stage B larger [ ] They are similar

because

ii) Which emitter follower stage has the larger <u>output resistance</u>, and why?

[ ] Stage A larger [ ] Stage B larger [ ] They are similar

because

iii) For which emitter follower stage has voltage gain closer to one, and why?

[ ] Stage A closer to 1 [ ] Stage B closer to 1 [ ] They are similar

because

Problem 1 continues on the next page

Problem 1 continued

e) [3 pts] An isolated n-type silicon sample with $N_D = 10^{17}$ cm^{-3}, minority carrier lifetime, τ_{min}, equal to 10^{-5} s, and perfectly reflecting boundaries (i.e., no surface recombination) has been illuminated for a long time with light generating 10^{20} hole-electron pairs/cm^3-s uniformly throughout its bulk. At t = 0 the light is extinquished. What is the excess minority carrier density in this sample as a function of time for $t \geq 0$?

.

$p'(t \geq 0) =$ ______________________________ cm^{-3}

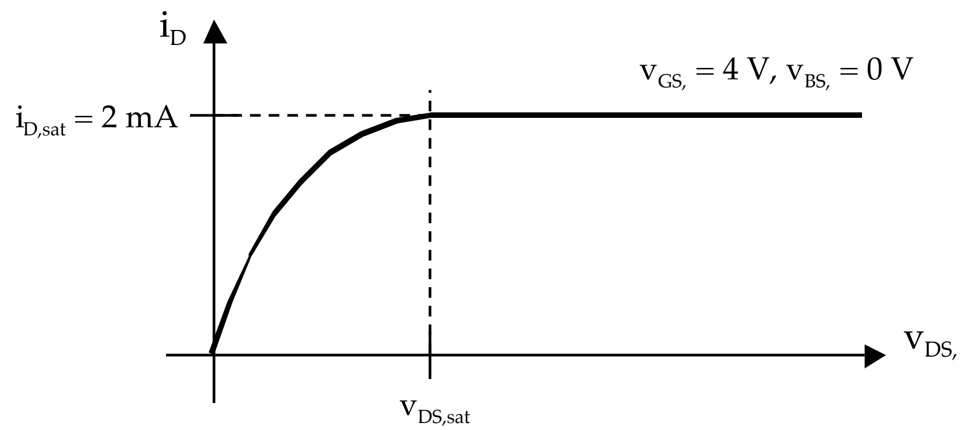
End of Problem 1

Problem 2 (25 points)

An ideal n-channel MOSFET has the i_D vs v_{DS} characteristic shown below when $v_{GS} = 4$ V and $v_{BS} = 0$ V. Note that the drain current saturates at 2 mA for $v_{DS} \geq V_{DS,sat}$.

The threshold voltage, $V_T(v_{BS})$ of this device is 1 V when $v_{BS} = 0$ V, i.e. $V_T(0) = 1$ V. It has the following structural parameters:

$N_A = 10^{17}$ cm^{-3}, W = 25 μm, L = 10 μm, $t_{ox} = 10^{-6}$ cm, and $\varepsilon_{ox} = 3.5 \times 10^{-13}$ F/cm



a) [3 pts] What is the drain-to-source saturation voltage, $v_{DS,sat}$, when $v_{GS} = 4$ V?

$v_{DS,sat}$ = ____________________V

b) [4 pts] Use the information provided to calculate the electron mobility, μ_e, in the channel.

μ_e = ______________________ cm^2/V-s

Problem 2 continues on the next page

Problem 2 continued

c) [5 pts] Find the inversion layer sheet charge density in the channel, $q_N^*(y)$, at the source end, i.e. $q_N^*(0)$, and at the drain end, $q_N^*(L)$, for the bias condition $V_{GS} = 4$ V, $V_{DS} = 1$ V, and $V_{BS} = 0$ V.

At the source end, $q_N^*(0) =$ ________________ Coul/cm^2

At the drain end, $q_N^*(L) =$ ________________ Coul/cm^2

d) [5 pts] Find the average net velocity, $\bar{s}_y(y)$, of the electrons in the channel at the source end, i.e. $\bar{s}_y(0)$, and at the drain end, $\bar{s}_y(L)$, for the bias condition in Part (c) above, for which the corresponding drain current, I_D, is 0.55 mA. If you could not solve Part (c) give an algebraic expression as your answer.

At the source end, $\bar{s}_y(0) =$ ________________ cm/s

At the drain end, $\bar{s}_y(L) =$ ________________ cm/s

Problem 2 continues on the next page

Problem 2 continued

e) [5 pts] The drain-to-source voltage, v_{DS}, is <u>increased</u> to 5 V, so that the bias condition is now $V_{GS} = 4$ V, $V_{DS} = 5$ V, and $V_{BS} = 0$ V. Find the inversion layer sheet charge density in the channel, $q_N^*(y)$, at the source end, i.e. $q_N^*(0)$, and at the drain end, $q_N^*(L)$ under this new bias condition.

At the source end, $q_N^*(0) =$ ________________ Coul/cm^2

At the drain end, $q_N^*(L) =$ ________________ Coul/cm^2

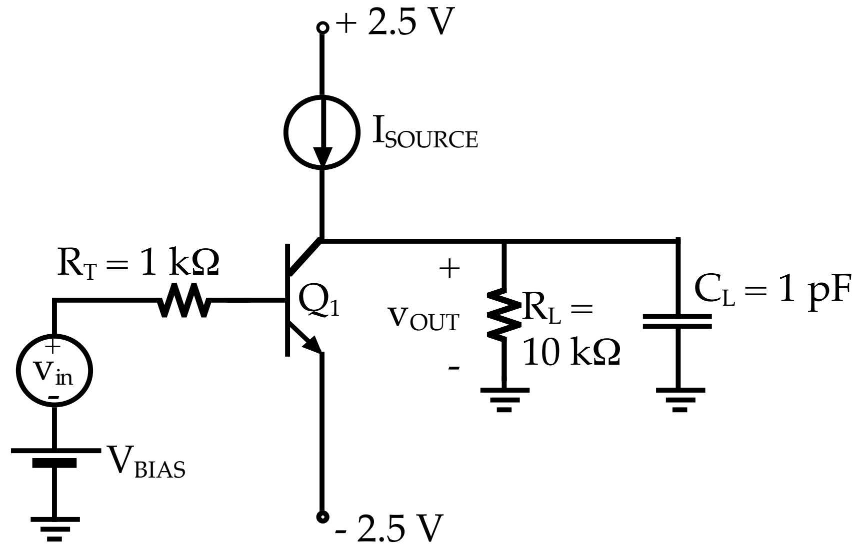
f) [3 pts] Next consider this MOSFET with a negative substrate-to-source bias, V_{BS}. What is the drain current of this device when it is biased in saturation, i.e., with $V_{DS} \geq (V_{GS} - V_T)$, with $V_{GS} = 4$ V and $V_{BS} = -5$ V?

$i_{D,sat} =$ ________________________ mA

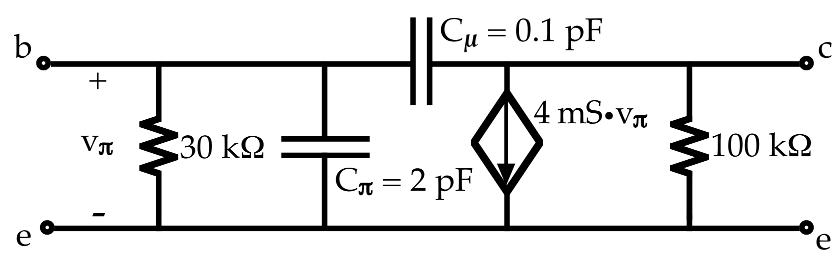
End of Problem 2

Problem 3 - (25 points)

A bipolar transistor, Q_1, is used in the voltage amplifier circuit below and biased in its forward active region. There is an ideal current source ($g_o = 0$) with a current output of I_{SOURCE} in the collector leg of the circuit, and the bias voltage on the base, V_{BIAS}, is adjusted to that the quiescent output voltage, V_{OUT}, is 0 Volts. For Q_1, $V_{BE,on}$ = 0.6 V and $V_{CE,sat}$ = 0.2 V.



The schematic below shows the small-signal linear equivalent circuit model for Q_1. The element values stated are correct for the bias point in the circuit above.



a) [4 pts] Use the information in the linear equivalent circuit to find the quiescent collector current and calculate the value of I_{SOURCE} that will give a quiescent output voltage, V_{OUT}, of 0 V.

I_{SOURCE} = ____________ mA

Problem 3 continues on the next page

Problem 3 continued

b) [4 pts] What is the forward current gain, β_F, of Q_1?

β_F = ________________

c) [4 pts] What is the Early voltage, V_A, of Q_1?

V_A = ________________ Volts

d) [4 pts] Which of the three capacitors in the circuit, C_π, C_μ, or C_L, is in the Miller position, and what is its effective value across the base-emitter terminals of Q_1, as a result of the Miller effect?

[ ] C_π [ ] C_μ [ ] C_L is in the Miller position because

Effective capacitance, C_{Eff} =________________ pF

e) [6 pts] Using the open circuit time constant technique and the Miller Approximation, calculate the time constant associated with each of the three capacitors, C_π, C_μ, and C_L.

(i) C_π:

τ_π =________________ s

Problem 3 continues on the next page

Problem 3 continued

e) cont.

(ii) C_μ:

τ_μ =__________________ s

(iii) C_L:

τ_L =__________________ s

f) [3 pts] Estimate the bandwidth, f_{BW}, of this amplifier (in Hz).

f_{BW} =__________________ Hz

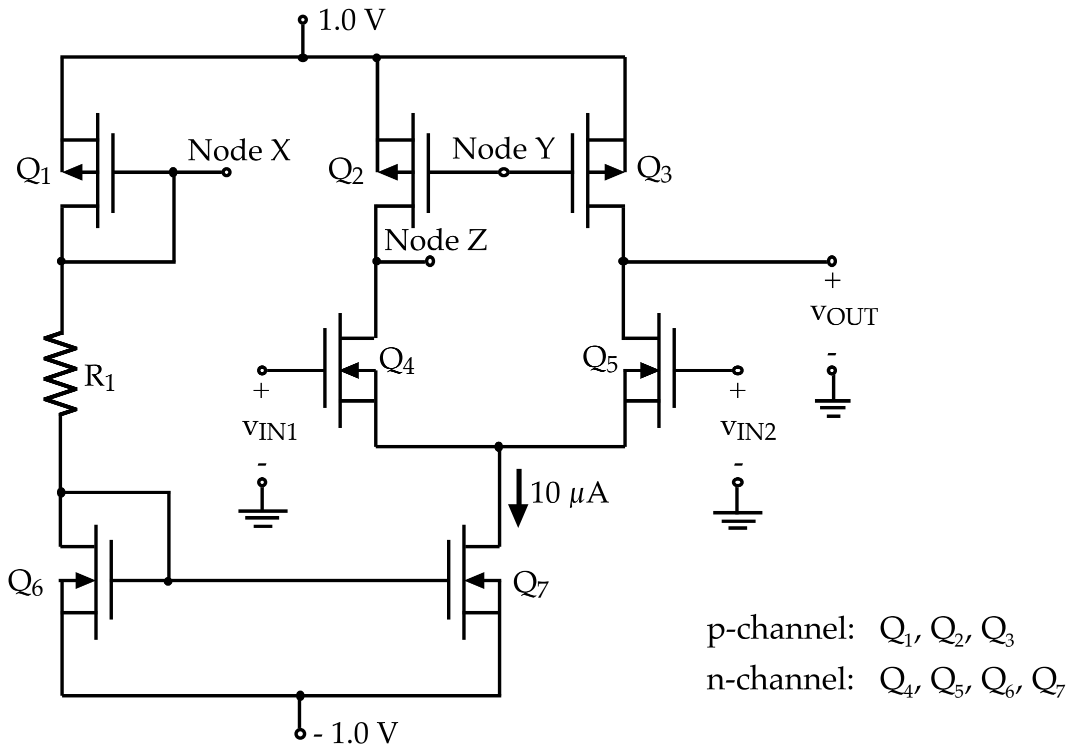
End of Problem 3

Problem 4 - (25 points)

The circuit shown below contains n-channel and p-channel MOSFETs all of which have the same gate length, $L = L_{min}$; all the gate widths are not equal, however they are all <u>integer multiples</u> of W_{min}. The magnitude of all the MOSFETs' Early voltages, $|V_A|$, is 10 V; the magnitude of all of their threshold voltages, $|V_T|$, is 0.5 V; and all must be biased with $|V_{GS} - V_T| \geq 0.1$ V.

The supply voltages are + 1 V and - 1 V.

The K-factor of an n-channel MOSFET with $L = L_{min}$ and $W = W_{min}$ is 500 $\mu A/V^2$, and the K-factor of a p-channel MOSFET with $L = L_{min}$ and $W = W_{min}$ is 250 $\mu A/V^2$.



The drain current of Q_7 is known to be 10 μA, and the width of Q_6, W_6, is known to be W_{min}. The resistor R_1 has been selected so that Q_1 and Q_6 are biased with $|V_{GS} - V_T| = 0.1$ V. The widths of Q_2, Q_3, Q_4, and Q_5 have been chosen so that they are also all biased with $|V_{GS} - V_T| = 0.1$ V, i.e., when $v_{IN1} = v_{IN2} = 0$.

<u>For Parts a), b), c) and d) connect Node Y to Node X</u>.

a) [6 pts] This part concerns the bias chain Q_1, R_1, and Q_6.

(i) What is I_{D6}, the drain current of Q_6?

I_{D6} = ________________ μA

Problem 4 continues on the next page

Problem 4 continued

a) cont.

(ii) What are W_1, and W_7, the widths of Q_1 and Q_7, respectively?

W_1 / W_{min} = ___________ (integer only)

W_7 / W_{min} = ___________ (integer only)

(iii) What is the value of the resistor R_1?

R_1 = _______________ Ω

b) [6 pts] What is the small signal output, v_{out}, with the following difference-mode inputs: $v_{in1} = v_a$ and $v_{in2} = -v_a$? Give your answer in three forms: (i) an expression in terms of the g_m's and g_o's of the relevant transistors, (ii) an expression in terms of the bias points of the relevant transistors, and (iii) a numerical value.

Remember that Node Y is connected to Node X.

(i) v_{out} (in terms of g_m's, g_o's)= _________________________ v_a

(ii) v_{out} (in terms of quiescent values) = _________________________ v_a

(iii) v_{out} (numerical value) = _________________________ v_a

Problem 4 continues on the next page

Problem 4 continued

c) [3 pts] What is the most negative common mode voltage, v_{IC}, that can be applied to the input terminals before one or more transistors in the amplifier are forced out of saturation? Remember that Node Y is connected to Node X.

Most negative v_{IC} = ____________________ V

d) [4 pts] In the space provided below, draw the linear equivalent <u>half-circuit</u> for this amplifier for the following <u>common-mode</u> inputs: $v_{in1} = v_{in2} = v_b$. Label your drawings in terms of the g_m's and g_o's of the relevant transistors. You <u>do not</u> need to find numerical values for the elements. Recall that Node Y is connected to Node X.

e) [4 pts] How will your answers in Part b) change if <u>Node Y is connected to Node Z</u>, instead of to Node X? Give the name of this new connection, <u>and</u> give the ratio of the v_{out} with Y connected to Z, to that with v_{out} with Y connected to X.

Name = ________________________________

v_{out}(Y to Z)/ v_{out}(Y to X) ≈ ________________

f) [2 pts] What is the quiescent power dissipation, P_Q, in this circuit?

P_Q = ________________ μW

End of Problem 4; End of Final Exam; Have a great summer.