Quiz 1:

Time: Regular class time 1 Hour

1 HANDWRITTEN "Crib Sheet" allowed

Venue:

Problem Sets 1-3, Lab 1, Lectures 1-8 (e.g. to today)

General Topics:

Boolean Algebra and Elementary Logic:

Basic Expressions

(Rules of Boolean Algebra, Demorgan's Theorem)

Canonical Forms (Sum of Products, Product of Sums)

Minimal Expressions (MSP, MPS)

Karnaugh Maps for simple expressions

Relationship to logical circuit diagrams

Combinational Logic

TTL: Voltage and Current Levels

Synchronous and asynchronous logic

Timing: Combinatoric delay, clock to Q,

Setup and Hold times

Bus Mechanisms: Totem Pole, Open Collector, ...

More:...

Finite State Machines:

- **Transition Tables and Transition Diagrams**
- **Timing Diagrams**
- **Mealey and Moore Machines**

Building Blocks:

- **S-R Latches**
- **Edge Triggered Devices**
- **Flip-Flops (D, T, JK)**
- **MUXes, deMUXes (selectors)**
- **Counters**

PALs

- **Internal Architecture: SP realization**
- **Clock and OE realizations**
- **Don't worry about specifics for specific parts**

VHDL:

- **Understand logical assignment, instantiation**
- **IF/Then/Else and Case/When statement structures**
- **Entity and Architecture**