

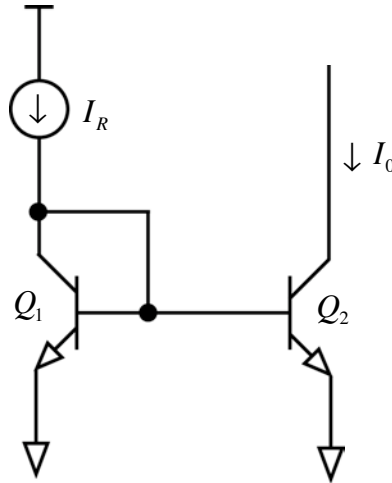
## 6.301 Solid-State Circuits

Recitation 14: Op-Amps and Assorted Other Topics

Prof. Joel L. Dawson

---

First, let's take a moment to further explore device matching for current mirrors:



and ask what happens when  $Q_1$  and  $Q_2$  operate at different temperatures. It turns out that grinding through the math doesn't yield a great deal of insight:

$$\frac{I_1}{I_2} = \frac{I_{S1} \exp\left[\frac{qV_{BE}}{kT_1}\right]}{I_{S2} \exp\left[\frac{qV_{BE}}{kT_2}\right]} = \frac{I_{S1}}{I_{S2}} \exp\left[\frac{qV_{BE}}{k} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

We must consider, too that the saturation currents  $I_s$  are temperature-dependent as well. It turns out that  $I_s$  can be written

$$I_s = \frac{T^\gamma}{E} \exp\left(-\frac{qV_{G0}}{kT}\right)$$

Where  $E$ ,  $\gamma$  are constants and  $V_{G0}$  is the bandgap voltage. All I can say here is that if  $Q_1$  and  $Q_2$  are at different temperatures,  $I_1 \neq I_2$ . End of story.

## 6.301 Solid-State Circuits

Recitation 14: Op-Amps and Assorted Other Topics

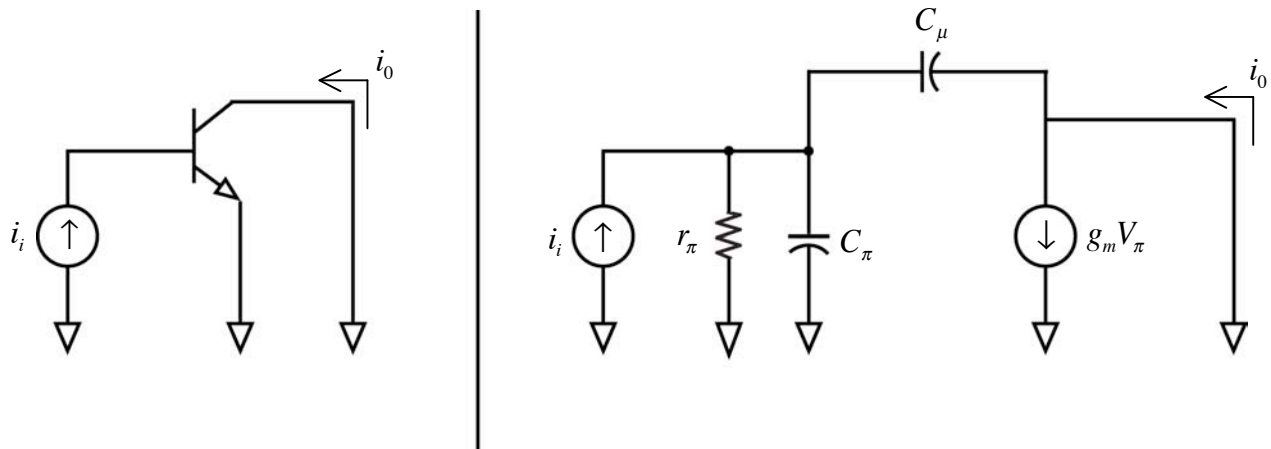
Prof. Joel L. Dawson

---

Next, let's take a moment to consider carefully a (true) statement that Prof. Roberge has made in class in previous semesters. I can't quote him exactly, but he said something like:

“When transistors are run at low collector currents, they tend to have low  $f_T$ s.”

What does this mean? Well,  $f_T$  concerns the result of the following experiment:



We ask ourselves, what is the frequency at which the current gain  $\left| \frac{i_o}{i_i} \right|$  falls to unity? That frequency is called the " $f_T$ " of transistor, and is given by the expression

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_\pi + C_\mu}$$

People quote this number as a general indication of how “fast” a transistor is. Generally speaking, it will be easier to design a high-bandwidth amplifier using a transistor with a higher, rather than lower  $f_T$ . Note that since the output is short-circuited, the Miller effect never comes into play. This causes  $C_\pi$  and  $C_\mu$  to be treated equally for the sake of  $f_T$ , but we know that for real voltage amplifiers  $C_\mu$  can be more painful.

## 6.301 Solid-State Circuits

Recitation 14: Op-Amps and Assorted Other Topics

Prof. Joel L. Dawson

---

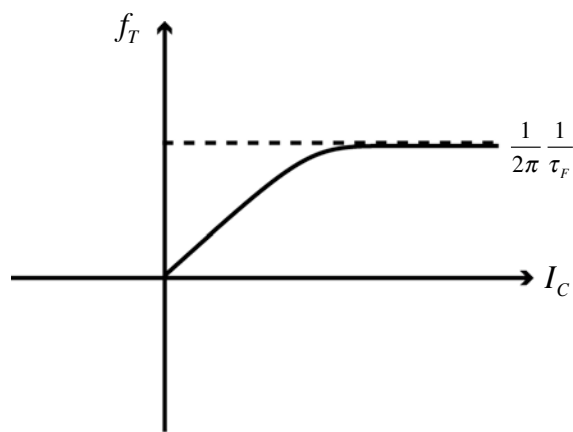
Looking at this expression, we can express parts of it in terms of the collector current  $I_C$ .

$$g_m = \frac{I_C}{V_T} \qquad C_\pi = g_m \tau_F + C_{je}$$

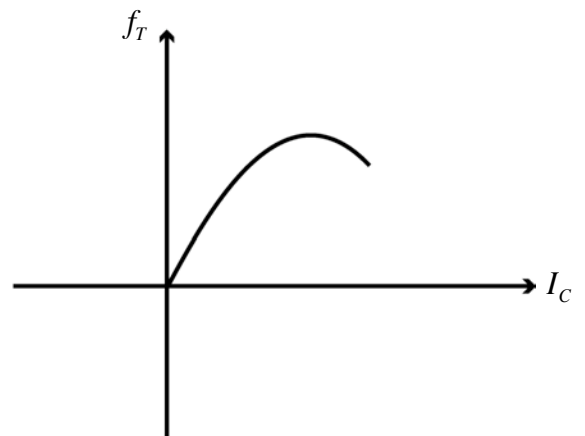
$$\qquad \qquad \qquad = \frac{I_C}{V_T} \tau_F + C_{je}$$

$$f_T = \frac{1}{2\pi} \frac{\frac{I_C}{V_T}}{\tau_F \frac{I_C}{V_T} + C_{je} + C_\mu}$$

We see that in the limit of  $I_C \rightarrow 0$ ,  $f_T \rightarrow 0$ , while in the limit of  $I_C \rightarrow \infty$ ,  $f_T \rightarrow \frac{1}{2\pi} \frac{1}{\tau_F}$ . Below is a sketch of  $f_T$  vs.  $I_C$  as predicted by this simple theory; next to it is a graph from a measured device.



Simple Theory



Reality

( $\beta_F$  tends to decay at high currents.)

---

Now, at last on to the class exercise.

## 6.301 Solid-State Circuits

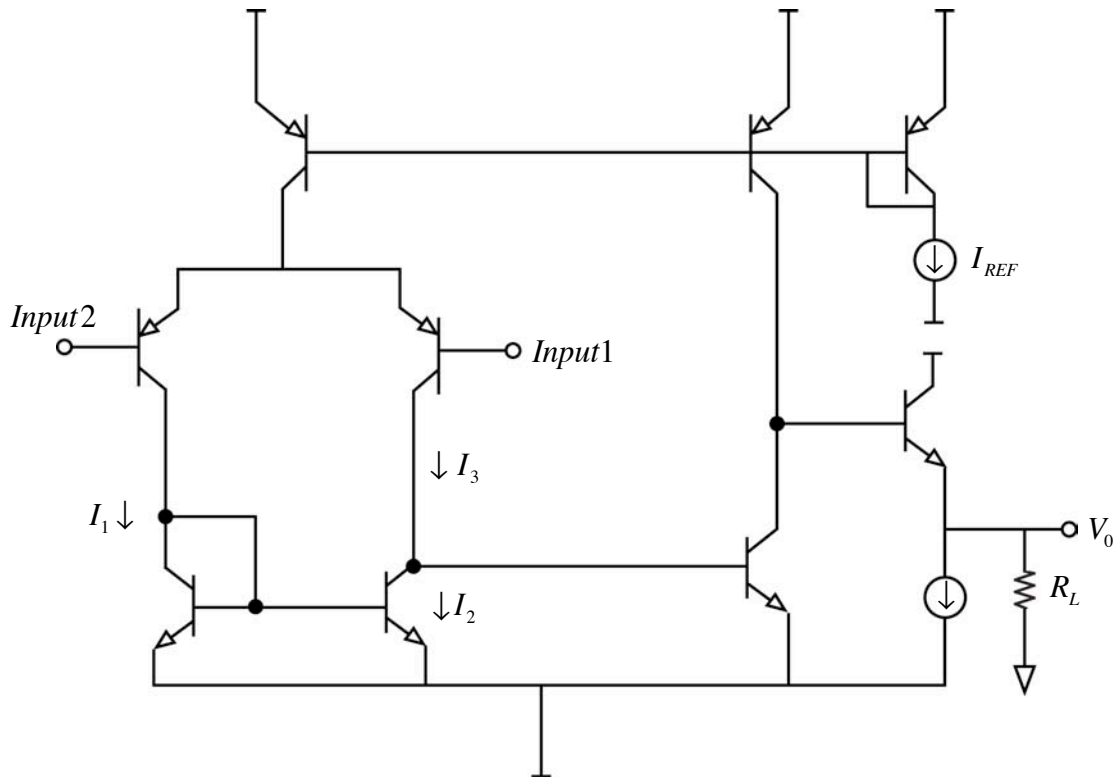
Recitation 14: Op-Amps and Assorted Other Topics

Prof. Joel L. Dawson

---

### CLASS EXERCISE

Consider the simple op-amp shown below. Which is the inverting input, and which is the non-inverting input?



This is a seemingly simple exercise, but tracing things through helps you begin to understand how these things are put together.

Now, notice that the input stage is loaded with a current mirror. We know, based on our knowledge of the “simple” current mirror, that  $I_1$  and  $I_2$  are related by

$$I_2 = \frac{I_1}{1 + \frac{2}{\beta}}$$

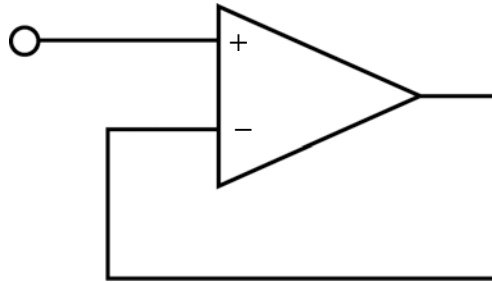
If the two inputs are the same (the differential input voltage is zero),  $I_1 = I_3$ . This means that  $I_3 \neq I_2$  ... which means trouble? Fortunately not. This is one of those cases where the designer relies on the op-amp being in a feedback connection. Take, for example, a follower:

## 6.301 Solid-State Circuits

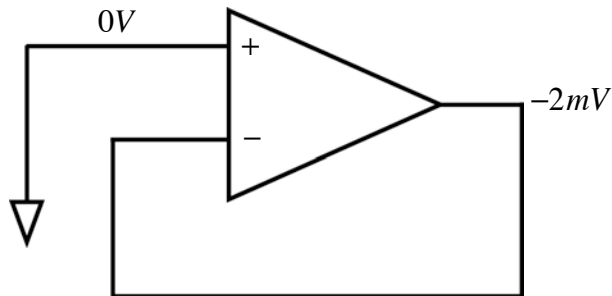
Recitation 14: Op-Amps and Assorted Other Topics

Prof. Joel L. Dawson

---



In the op-amp on the last page, we expect  $I_2 < I_3$  for zero differential input. Connected as above, though, this would drive the output, and therefore the inverting input, low. When the inverting input is drawn low, it causes  $I_2$  to increase. The system quickly equilibrates to  $I_2 \approx I_3$ , and if we measure the voltages we might measure something like:



---

Particularly in ICs it is not uncommon to implement an entire op-amp in a single stage. There are many tricks for getting a lot of gain. It is sometimes useful to use cascoding to establish very high-impedance nodes.

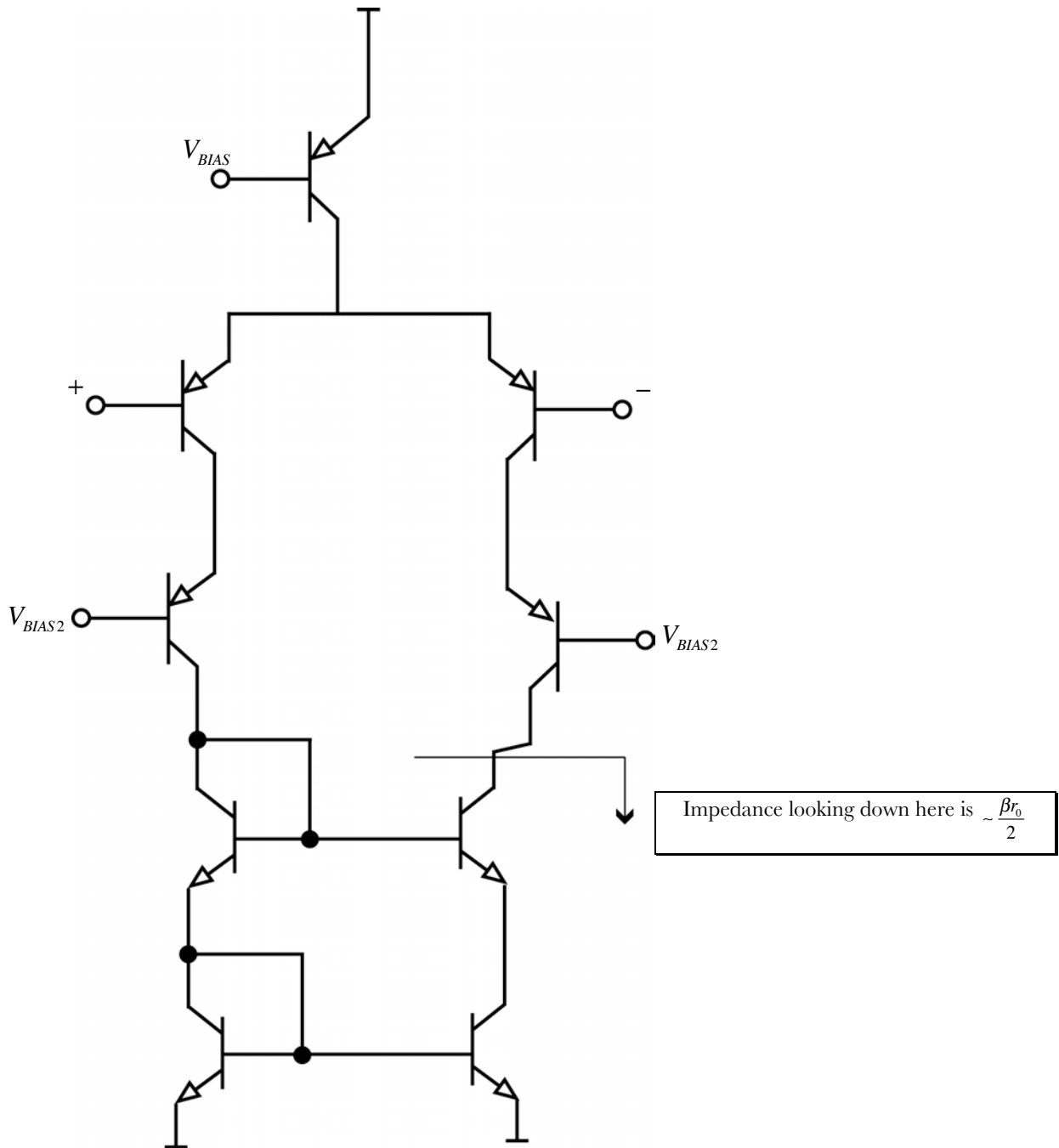
## 6.301 Solid-State Circuits

Recitation 14: Op-Amps and Assorted Other Topics

Prof. Joel L. Dawson

---

Input stage that could be used for very high gain:



This concept is more commonly used with MOSFETS, especially in situations when you expect to drive a purely capacitive load.

MIT OpenCourseWare  
<http://ocw.mit.edu>

6.301 Solid-State Circuits  
Fall 2010

For information about citing these materials or our Terms of Use, visit: <http://ocw.mit.edu/terms>.