6.334 Power Electronics
Spring 2007

Chapter 5

Introduction to DC/DC Converters

Analysis techniques: Average KVL, KCL, P.S.S. Conditions.

KCL

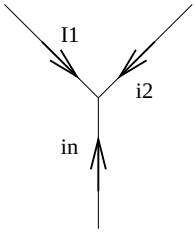

Figure 5.1: KCL

$$\sum i_j = 0 \tag{5.1}$$

Average over time:

$$\begin{aligned} \frac{1}{T}\int_T \sum i_j &= 0 \\ \sum \frac{1}{T}\int_T i_j &= 0 \\ \sum < i_j > &= 0 \end{aligned} \tag{5.2}$$

KCL applies to average current as well as instantaneous currents. (Derives from conservation of charge).

KVL

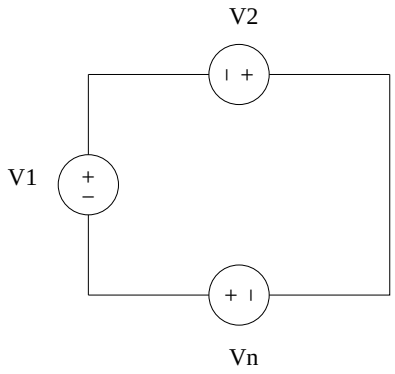

Figure 5.2: KVL

$$\sum V_k = 0 \tag{5.3}$$

Average over time:

$$\begin{aligned} \frac{1}{T}\int_T \sum V_k &= 0 \\ \sum \frac{1}{T}\int_T V_k &= 0 \\ \sum < V_k > &= 0 \end{aligned} \tag{5.4}$$

KVL applies to averaged variables.

P.S.S.

To analyze converters in Periodic Steady State (P.S.S.):

$$\text{Average KCL} \quad \sum < i_j > \;=\; 0 \tag{5.5}$$

$$\text{Average KVL} \quad \sum < V_k > \;=\; 0 \tag{5.6}$$

$$\text{from } < V_L > \;=\; L < \frac{di_L}{dt} >$$

$$\text{in P.S.S.} \quad < \frac{di_L}{dt} > \;=\; 0$$

$$\text{Inductor in P.S.S.} \quad < V_L > \;=\; 0 \tag{5.7}$$

$$\text{from } < i_C > \;=\; C < \frac{dV_L}{dt} >$$

$$\text{in P.S.S.} \quad < \frac{dV_L}{dt} > \;=\; 0$$

$$\text{Capacitor in P.S.S.} \quad < i_C > \;=\; 0 \tag{5.8}$$

$$\text{If Circuit is Lossless:} \quad P_{in} \;=\; P_{out} \tag{5.9}$$

Consider the DC/DC converter from before (see Figure 5.3):

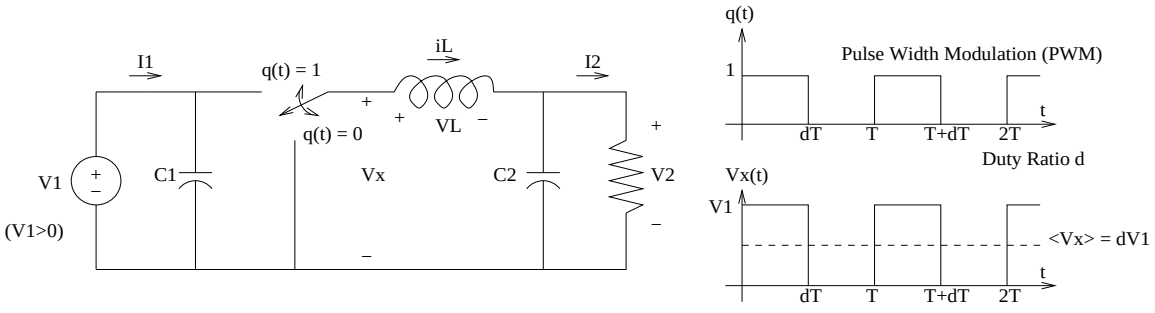

Figure 5.3: DC/DC Converter

Assume L's and C's are very big, therefore:

$$v_C(t) \simeq V_C \tag{5.10}$$

$$i_L(t) \simeq I_L \tag{5.11}$$

Analyze (using average relations) in P.S.S.:

$$\begin{aligned} < V_L > &= 0 \\ < V_L > &= dT(V_1 - V_2) + (1-d)T(-V_2) \\ dV_1T - V_2T &= 0 \\ V_2 &= dV_1 \end{aligned} \tag{5.12}$$

(Since $< V_L >= 0, \quad < V_2 >=< V_x >= dV_1$.)

Consider currents:

$$\begin{aligned} < i_{C2} > &= 0 \\ I_1 &= I_2 \end{aligned} \tag{5.13}$$

$$\begin{aligned} < i_{C1} > &= 0 \\ I_{C1} &= (I_1 - I_2 dT) + I_1(1-d)T = 0 \\ I_1 &= dI_2 \end{aligned} \tag{5.14}$$

Combining:

$$\begin{aligned} I_1 &= dI_2 \\ dV_1 &= V_2 \\ dV_1I_1 &= dI_2V_2 \\ V_1I_1 &= I_2V_2 \end{aligned} \tag{5.15}$$

Therefore, power is (ideally) conserved.

Note: Trick in this type of "average" analysis is to be careful when one can use an average value and when one must consider instantaneous quantities.

With the following type of external network and $V_1, V_2 > 0$, power flows from $1 \rightarrow 2$.

Switch implementation: "buck" or "down" converter (see Figure 5.4).

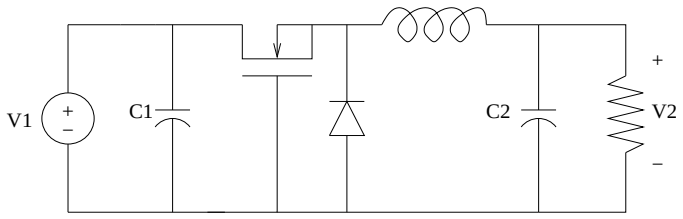

Figure 5.4: Buck (down) Converter

Type of "direct" converter because a DC path exists between input and output in one switch state.

Suppose we change the location of source and load: Refine switching function so $q(t) = 1$ when switch is in down position (see Figure 5.5).

Similar analysis:

$$\begin{aligned} < V_L > &= 0 \\ (V_1 - V_2)(1-d)T + V_1 dT &= 0 \\ V_2 &= \frac{1}{1-d} V_1 \end{aligned} \tag{5.16}$$

By conservation of power:

$$I_2 = (1-d) I_1 \tag{5.17}$$

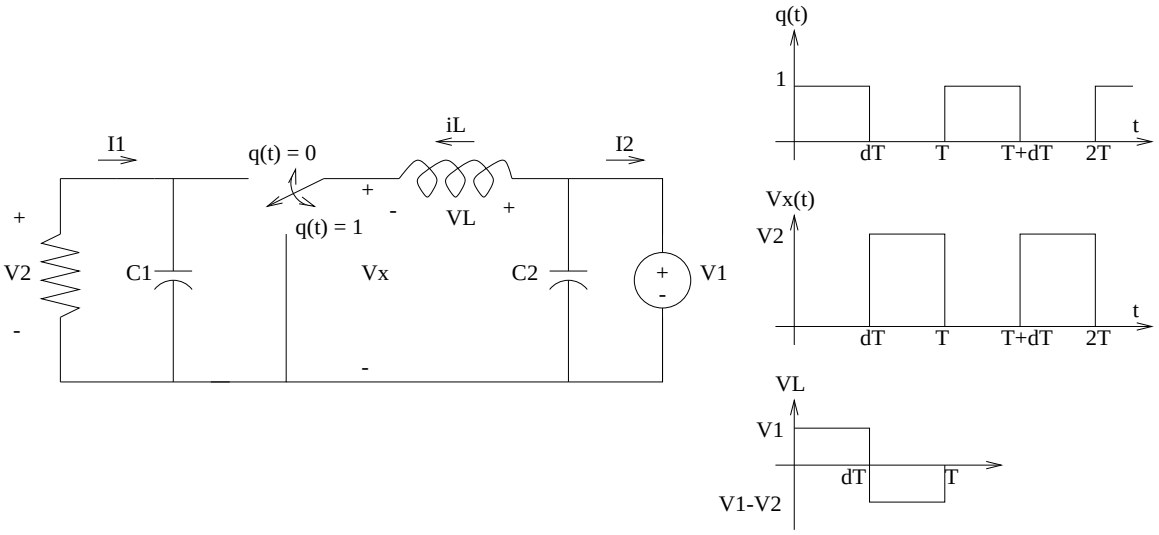

Figure 5.5: Change the Location of Source and Load

In this case, energy flows from $2 \leftarrow 1$ and the P.S.S. output voltage (V_2) is higher than input voltage (V_1).

With the following switch implementation: "boost" or "up" converter. Another type of "direct" converter (see Figure 5.6).

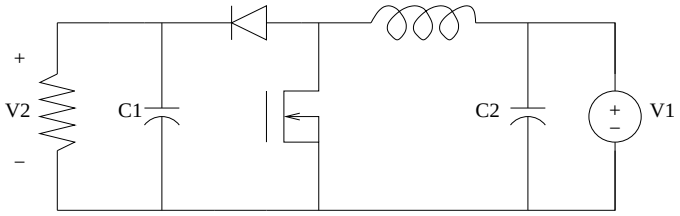

Figure 5.6: Boost (up) Converter

In general power flows direction depends on:

1. External network

2. Switch implementation

3. Control

We may need to know all of these to determine behavior.

The boost converter is often drawn with power flowing left to right. However, there is nothing fundamental about this (see Figure 5.7).

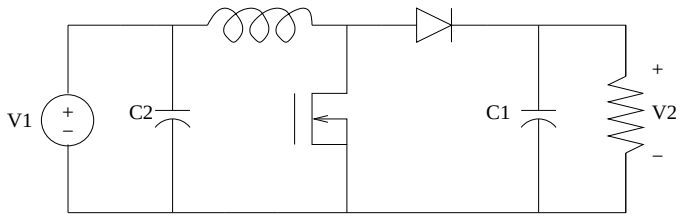

Figure 5.7: Boost (up) Converter Drawn Left to Right

Boost: Switch turns on and incrementally stores energy from V_1 in L. Switch truns off and this energy and additional energy from input is transferred to output. Therefore, L used as a temporary storage element.

Either the buck or boost can be seen as the appropriate connection of a canonical cell (see Figure 5.8).

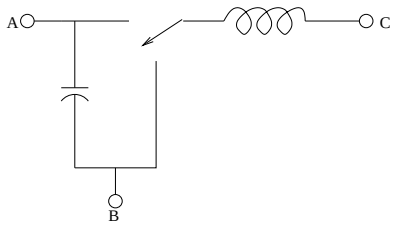

Figure 5.8: Direct Canonical Cell

The "direct" connection has B as the common node. The rest of operation is determined by external network, switch implementation and control.

Switch implementation: Different switches can carry current and block voltage only in certain directions.

MOSFET can block positive V and can carry positive or negative i (see Figure 5.9).

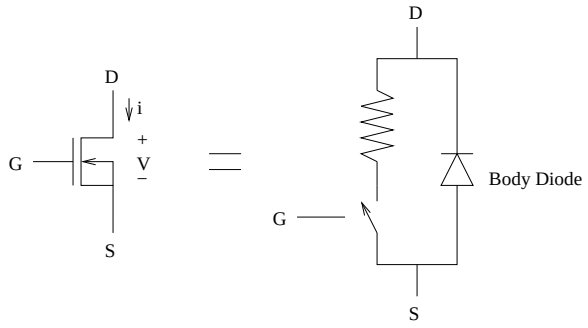

Figure 5.9: MOSFET

BJT (or darlington) is similar, but negative V blows up device (see Figure 5.10).

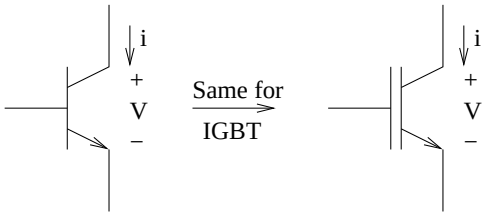

Figure 5.10: BJT

Combine elements:

1. Block positive V and carry positive and negative i (see Figure 5.11).

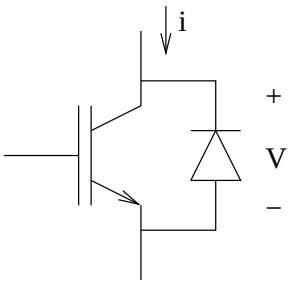

Figure 5.11: Combine Elements 1

2. Block positive and negative V and carry positive i (see Figure 5.12).

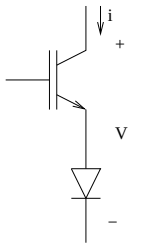

Figure 5.12: Combine Elements 2

3. Block positive and negative V and carry positive and negative i (see Figure 5.13).

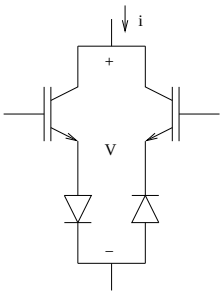

Figure 5.13: Combine Elements 3

We can also construct indirect DC/DC converters. Store energy from input, transfer energy to output, never a DC path from input to output (see Figure 5.14).

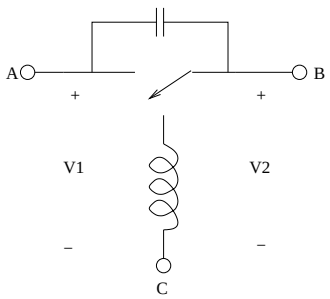

Figure 5.14: Canonical Cell

Split capacitor (see Figure 5.15):

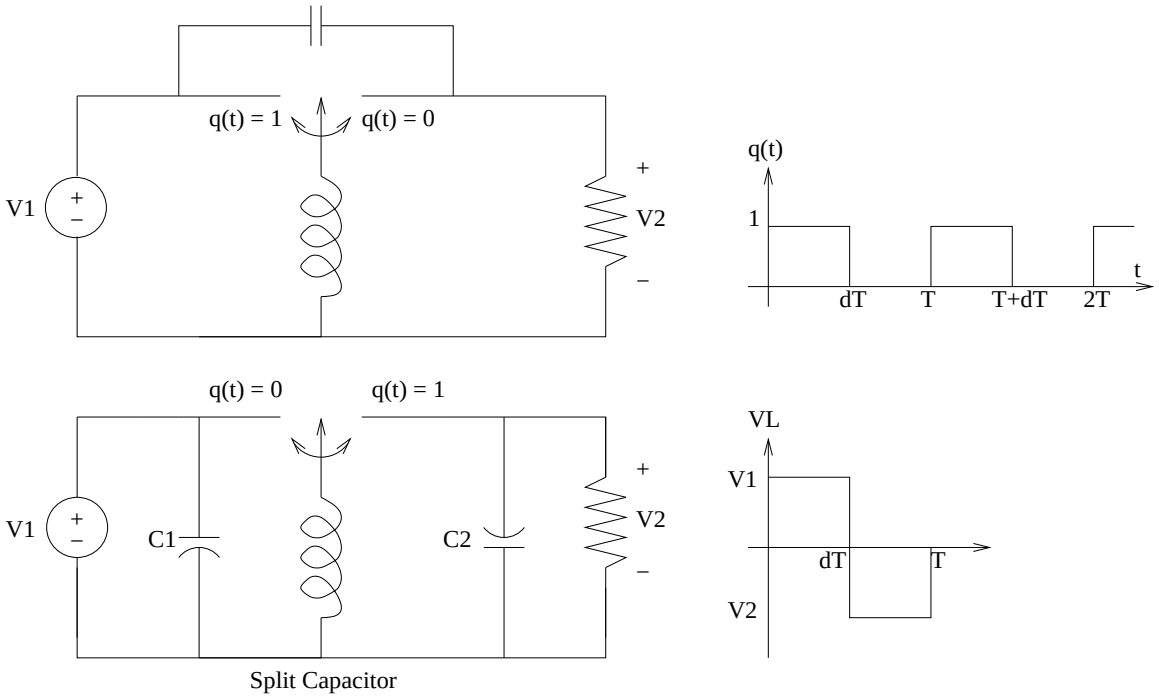

Figure 5.15: Indirect DC/DC Converter

$$\begin{aligned} < V_L > &= 0 \\ < V_L > &= V_1 dT + (1-d)TV_2 \\ V_2 &= -\frac{d}{1-d}V_1 \end{aligned} \tag{5.18}$$

$$for\ 0 < d < 1 \rightarrow -\infty < \frac{V_2}{V_1} < 0 \tag{5.19}$$

- Store energy in $L(dT)$ from V_1.
- Discharge it (the other way) in V_2. (must have voltage inversion).

"Buck/Boost" or "up/down" converter (see Figure 5.16):

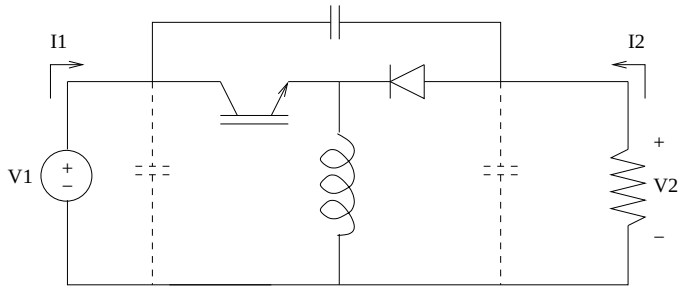

Figure 5.16: "Buck/Boost" or "up/down" converter

$$\begin{aligned} V_1 &> 0 \\ I_1 &> 0 \\ V_2 &< 0 \\ I_2 &> 0 \end{aligned}$$

Other indirect converters include CUK and SEPIC variants.

Given conversion range $-\infty < \frac{V_2}{V_1} < 0$, why not always use indirect vs. direct?

1. Sign inversion (can fix)

2. Device and component stresses

Look at averaged circuit variables (see Figure 5.17): Assume C, L are very large.

$$\begin{aligned} I_L &= I_1 + I_2 \\ |I_L| &= |I_1| + |I_2| \end{aligned} \tag{5.20}$$

By averaged KCL into dotted box: Maybe counter intuitive: I_1 = average transistor current. $I_1 + I_2$ = peak transistor current.

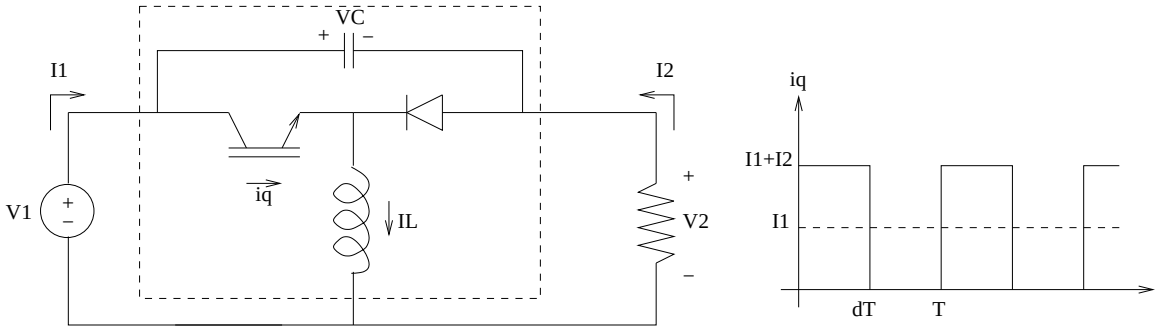

Figure 5.17: Averaged Circuit Variables

By averaged KVL around loop:

$$\begin{aligned} V_C &= V_1 - V_2 \\ |V_C| &= |V_1| + |V_2| \end{aligned} \tag{5.21}$$

Therefore, for big L, C (see Figure 5.18):

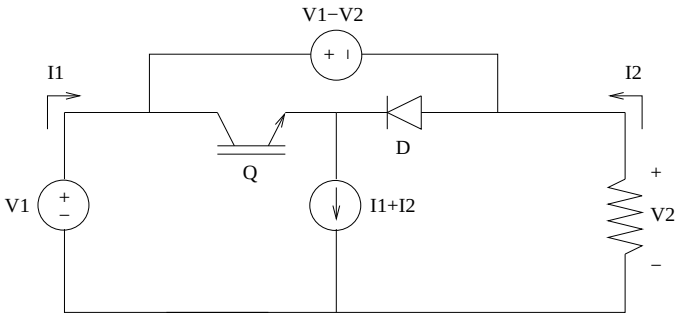

Figure 5.18: Big L, C

Indirect converter:

So Q, D, L see peak current $I = I_1 + I_2$,

Q, D, C block peak voltage $V = |V_1| + |V_2|$.

Consider direct converters (see Figure 5.19):

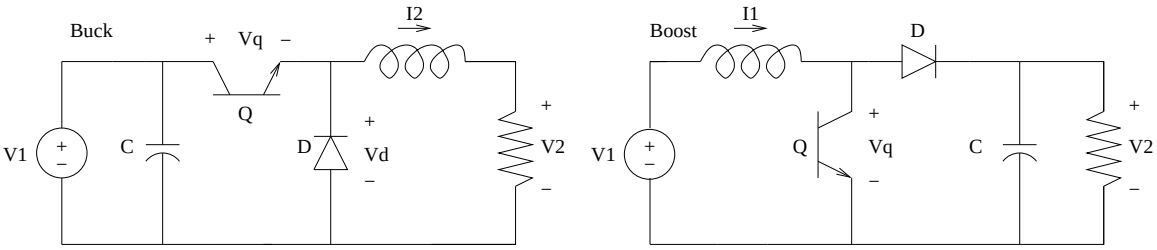

Figure 5.19: Direct Converters

Buck:

$$V_C = V_{q,max} = V_{d,max} = V_1 \tag{5.22}$$

$$I_L = i_{q,max} = i_{d,max} = I_2 \tag{5.23}$$

Boost:

$$V_C = V_{q,max} = V_{d,max} = V_2 \tag{5.24}$$

$$I_L = i_{q,max} = i_{d,max} = I_1 \tag{5.25}$$

Direct converters (either type):

$$V_C = V_{q,max} = V_{d,max} = \max(V_1, V_2) \tag{5.26}$$

$$I_L = i_{q,max} = i_{d,max} = \max(I_1, I_2) \tag{5.27}$$

Device voltage and current stresses are higher for indirect converters than for direct converters with same power. Inductor current and capacitor voltage are also higher.

Summary:

For indirect converters (neglecting ripple) (see Figure 5.20):

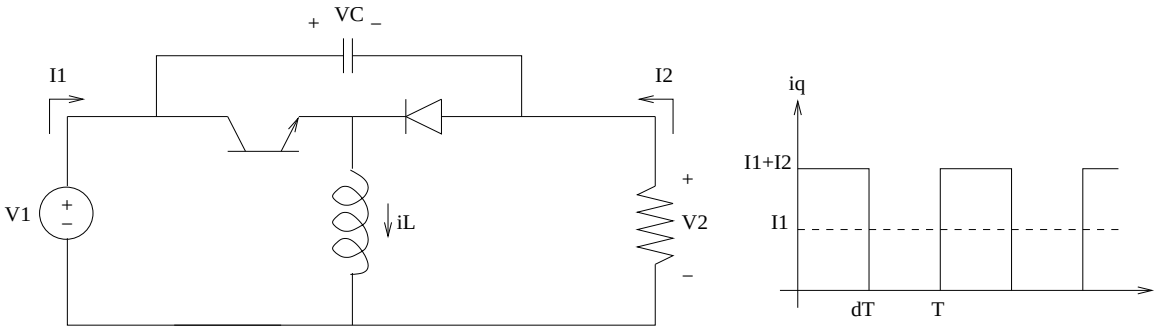

Figure 5.20: Indirect Converters (neglecting ripple)

$$I_L = i_{sw,pk} = i_{d,pk} = |I_1| + |I_2| \tag{5.28}$$

$$V_C = V_{sw,pk} = V_{d,pk} = |V_1| + |V_2| \tag{5.29}$$

For direct converters (neglecting ripple) (see Figure 5.21):

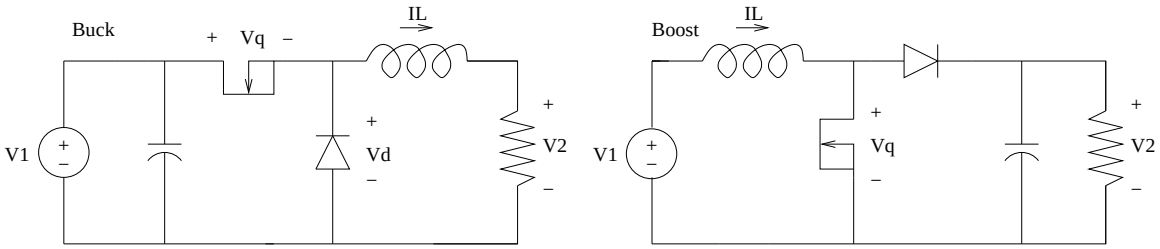

Figure 5.21: Direct Converters (neglecting ripple)

$$I_L = i_{sw,pk} = i_{d,pk} = \max(I_1, I_2) \tag{5.30}$$

$$V_C = V_{sw,pk} = V_{d,pk} = \max(V_1, V_2) \tag{5.31}$$

Based on device stresses we would not choose an indirect converter unless we needed to, since direct converters have lower stress.

5.1 Ripple Components and Filter Sizing

Now, selecting filter component sizes does depend on ripple, which we have previously neglected. Lets see how to approximately calculate ripple components. To eliminate 2^{nd} order effects on capacitor voltage ripple:

1. Assume inductor is $\infty(\Delta i_{pp} \to 0)$.

2. Assume all ripple current goes into capacitor.

Similarly, to eliminate 2^{nd} order effects in inductor current ripple:

1. Assume capacitors are $\infty(\Delta V_{C,pp} \to 0)$.

2. Assume all ripple voltage is across the inductor.

We can verify assumptions afterwards.

Example: Boost Converter Ripple (see Figure 5.22)

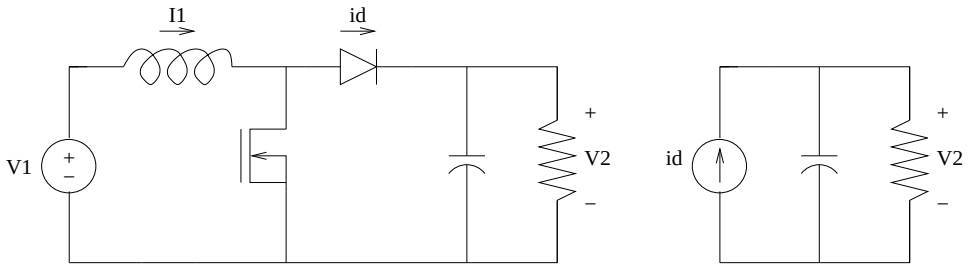

Figure 5.22: Boost Converter Ripple

Find capacitor (output) voltage ripple (see Figure 5.23):

Assume $L \to \infty$, therefore, $i_1(t) \to I_1$.

So a ripple model for the output voltage is (see Figure 5.24):

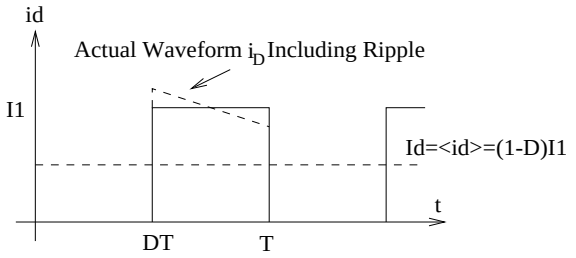

Figure 5.23: Capacitor Voltage Ripple

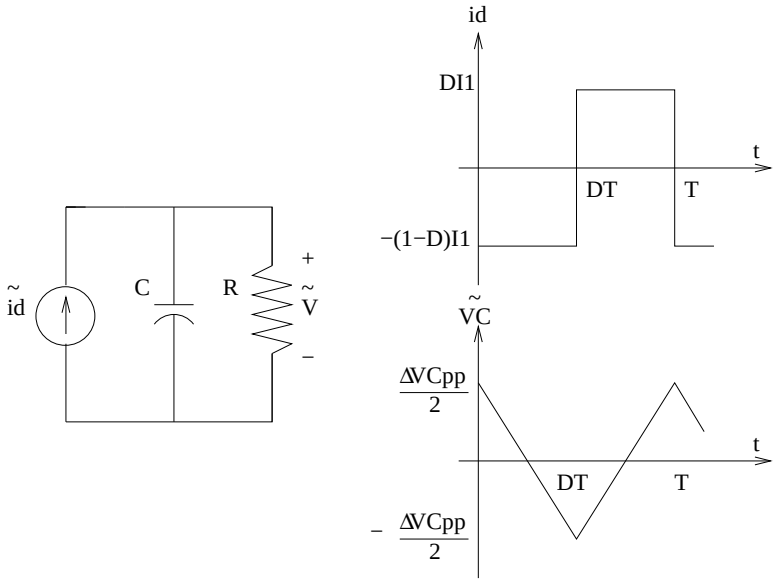

Figure 5.24: Ripple Model with Capacitor

If we assume all ripple current into capacitor $\frac{1}{2\pi f_{sw} C} \ll R$ or $\tilde{V_2}$ is small recpect to V_2.

Let us calculate the ripple:

$$\begin{aligned} i &= C\frac{dV_C}{dt} \\ \Delta V_{C,pp} &= \int_0^{DT} \frac{1-D}{C} I_1 dt \\ &= \frac{(1-D)DT}{C} I_1 \end{aligned} \tag{5.32}$$

Therefore, to limit ripple:

$$C \geq \frac{(1-D)DT}{\Delta V_{C,pp}} I_1 \tag{5.33}$$

Now let us find the capacitor voltage ripple (see Figure 5.25):

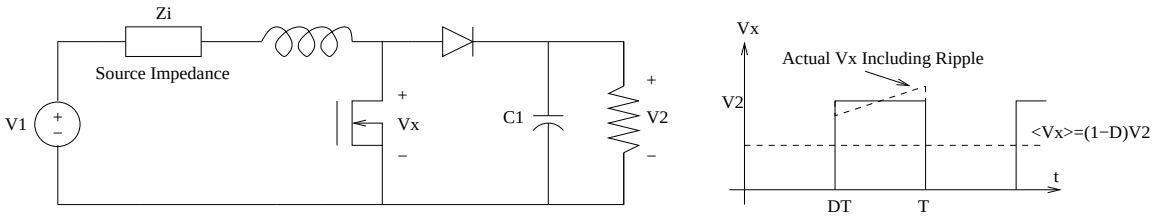

Figure 5.25: Ripple

Replace V_x with equivalent source and eliminate DC quantities (see Figure 5.26).

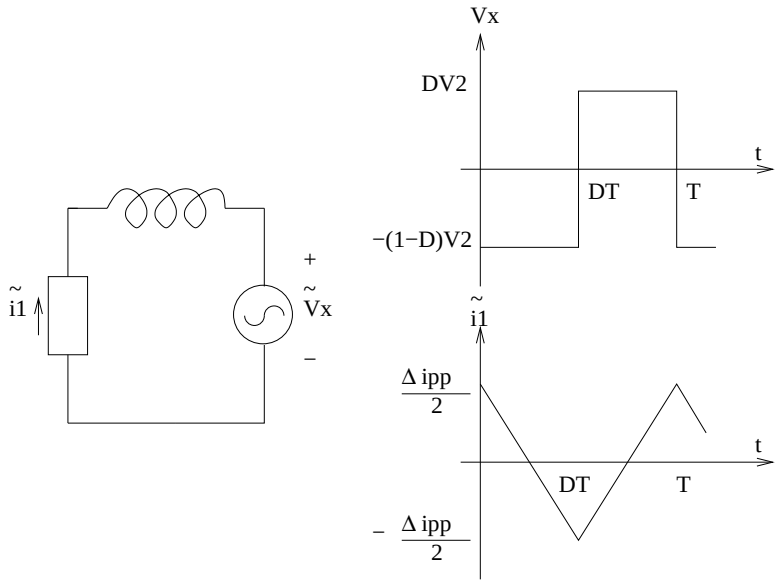

Figure 5.26: Ripple Model with Inductor

Neglecting the drop on any source impedance ($|Z_i| \ll 2\pi f_{sw} L$).

$$\begin{aligned} \Delta i_{L,pp} &= \frac{1}{L}\int_0^{DT} (1-D)V_2 dt \\ &= \frac{D(1-D)T}{L} V_2 \end{aligned} \tag{5.34}$$

Therefore, we need:

$$L \geq \frac{D(1-D)T}{\Delta i_{pp}} V_2 \tag{5.35}$$

Energy storage is one metric for sizing L's and C's. Physical size may actually be determined by one or more of: energy storage, losses, packing constraints, material properties. To determine peak energy storage requirements we must consider the ripple in the waveforms.

Define ripple ratios (see Figure 5.27):

$$\mathcal{R}_C = \frac{\Delta V_{C,pp}}{2V_C} \tag{5.36}$$

$$\mathcal{R}_L = \frac{\Delta i_{L,pp}}{2I - L} \tag{5.37}$$

This is essentially % ripple: peak ripple magnitude normalized to DC value.

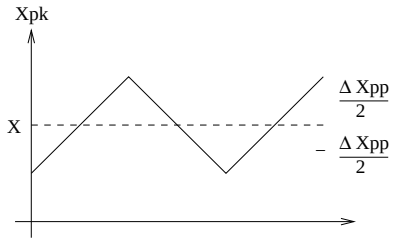

Figure 5.27: Ripple Ratios

Specification of allowed ripple and converter operating parameters determines capacitor and inductor size requirements.

Therefore:

$$V_{C,pk} = V_C(1 + \mathcal{R}_C) \tag{5.38}$$

$$i_{L,pk} = I_L(1 + \mathcal{R}_L) \tag{5.39}$$

So from our previous results (boost converter):

$$C \geq \frac{(1-D)DT}{2\mathcal{R}_C V_C} I_1 \tag{5.40}$$

$$L \geq \frac{D(1-D)T}{2\mathcal{R}_L I_1} V_2 \tag{5.41}$$

The ripple ratios also determine passive component energy storage requirements and semiconductor device stresses.

So lets calculate the required energy storage for the capacitor:

$$\begin{aligned} E_C &= \frac{1}{2} C V_{C,pk}^2 \\ &= \frac{1}{2} \frac{(1-D)DT}{2\mathcal{R}_C V_C} I_1 V_C^2 (1+\mathcal{R}_C)^2 \\ &= \frac{D I_2 V_2}{4 f_{sw}} \frac{(1+\mathcal{R}_C)^2}{\mathcal{R}_C} \\ &= \frac{D P_o}{4 f_{sw}} \frac{(1+\mathcal{R}_C)^2}{\mathcal{R}_C} \end{aligned} \tag{5.42}$$

So required capacitor energy storage increases with:

1. Conversion ratio

2. Power level

and decreases with switching frequency.

Similar result for inductor energy storage:

$$E_L = \frac{(1-D)P_o}{4 f_{sw}} \frac{(1+\mathcal{R}_L)^2}{\mathcal{R}_L} \tag{5.43}$$

It can be shown that direct converters always require lower energy storage than indirect converters.

Table 5.1: Effect of Allowed Ripple on Switches

Converter Type	**Value**	$L, C \to \infty$	**Finite** L, C
Direct	$i_{sw,pk}, i_{d,pk}$	$max(\|I_1\|, \|I_2\|)$	$max(\|I_1\|, \|I_2\|)(1+\mathcal{R}_L)$
	$V_{sw,pk}, V_{d,pk}$	$max(\|V_1\|, \|V_2\|)$	$max(\|V_1\|, \|V_2\|)(1+\mathcal{R}_C)$
Indirect	$i_{sw,pk}, i_{d,pk}$	$\|I_1\|, \|I_2\|$	$(\|I_1\|, \|I_2\|)(1+\mathcal{R}_L)$
	$V_{sw,pk}, V_{d,pk}$	$\|V_1\|, \|V_2\|$	$(\|V_1\|, \|V_2\|)(1+\mathcal{R}_C)$

Consider effect of allowed ripple on switches (see Table 5.1):

Define a metric for switch sizing (qualitative only):

$$Switch\ Stress\ Parameter(SSP) \doteq V_{sw,pk} i_{sw,pk} \tag{5.44}$$

For a boost converter:

$$\begin{aligned} SSP &= max(V_1, V_2)(1+\mathcal{R}_C) max(I_1, I_2)(1+\mathcal{R}_L) \\ &= V_2(1+\mathcal{R}_C) I_1(1+\mathcal{R}_L) \\ &= \frac{P_o}{1-D}(1+\mathcal{R}_C)(1+\mathcal{R}_L) \\ &= P_o \frac{V_2}{V_1}(1+\mathcal{R}_C)(1+\mathcal{R}_L) \end{aligned} \tag{5.45}$$

Therefore, SSP gets worse for:

- Large power
- Large conversion ratio
- Large ripple

5.2 Discontinuous Conduction Mode

Consider the waveform of the boost converter (see Figure 5.28):

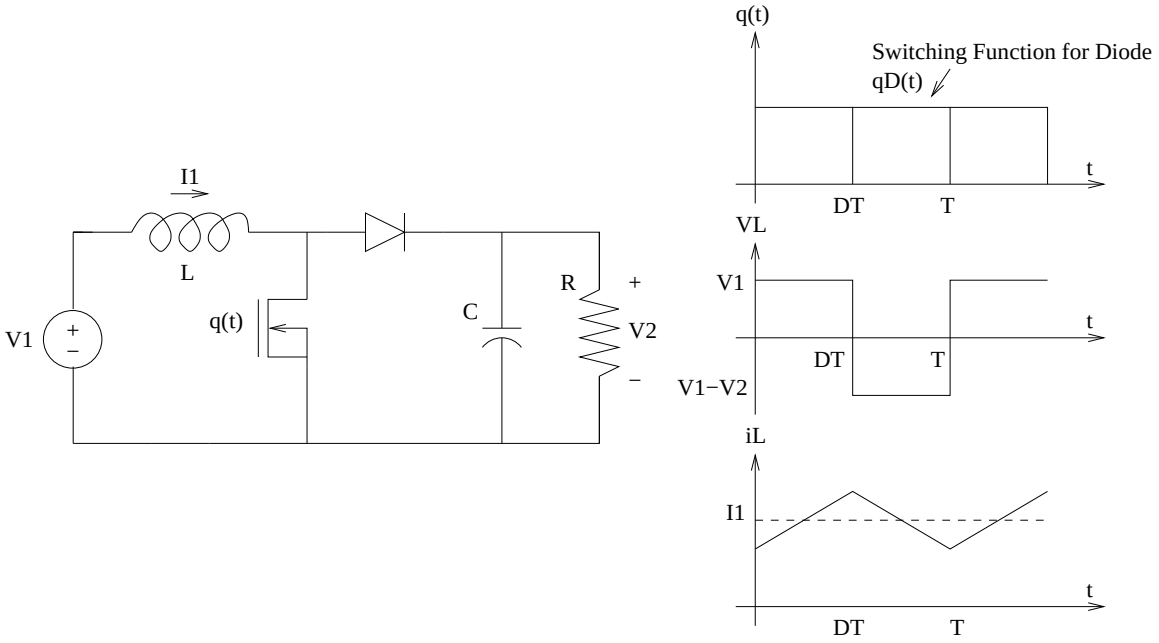

Figure 5.28: Boost Converter Waveforms

$$\Delta i_{L,pp} = \frac{V_1 DT}{L} \tag{5.46}$$

$$\begin{aligned} I_L &= I_1 \\ &= \frac{V_2}{R(1-D)} \end{aligned} \tag{5.47}$$

$$\begin{aligned} \mathcal{R}_L &= \frac{\frac{\Delta i_{L,pp}}{2}}{I_1} \\ &= \frac{V_1 D(1-D)RT}{2V_2 L} \\ &= \frac{D(1-D)^2 RT}{2L} \end{aligned} \tag{5.48}$$

$$\mathcal{R}_L \uparrow \ \ as\ R \uparrow, L \downarrow \tag{5.49}$$

(see Figure 5.29 for an illustration)

Eventually peak ripple becomes greater than DC current: both switch and diode off for part of cycle. This is known as Discontinuous Condition Mode (DCM). It

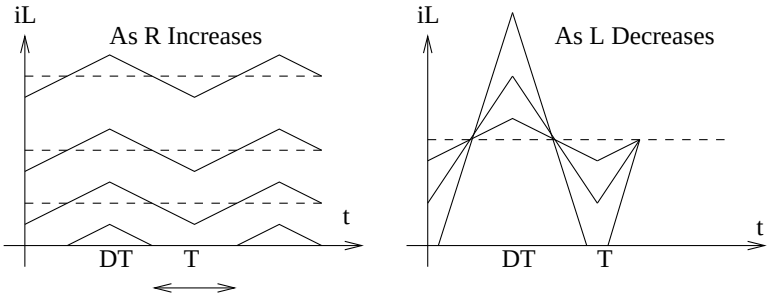

Figure 5.29: Changing R and L

happens when $\mathcal{R}_L > 1$.

$$\begin{aligned} \mathcal{R}_L &= \frac{D(1-D)^2RT}{2L} \\ \mathcal{R}_L &> 1 \\ R &\geq \frac{2L}{D(1-D)^2T} \end{aligned} \tag{5.50}$$

At light load (big R and low power) we get DCM. Lighter load can be reached in CCM for larger L. DCM occurs for:

$$L \leq \frac{D(1-D)^2TR}{2} \tag{5.51}$$

The minimum inductance for CCM operation is sometimes called the "critical inductance".

$$L_{CRIT,BOOST} = \frac{D(1-D)^2TR}{2} \tag{5.52}$$

For some cases (e.g. we need to operate down to almost no load), this may be unreasonably large.

Because of the new switch state, operating conditions are different (see Figure 5.30).

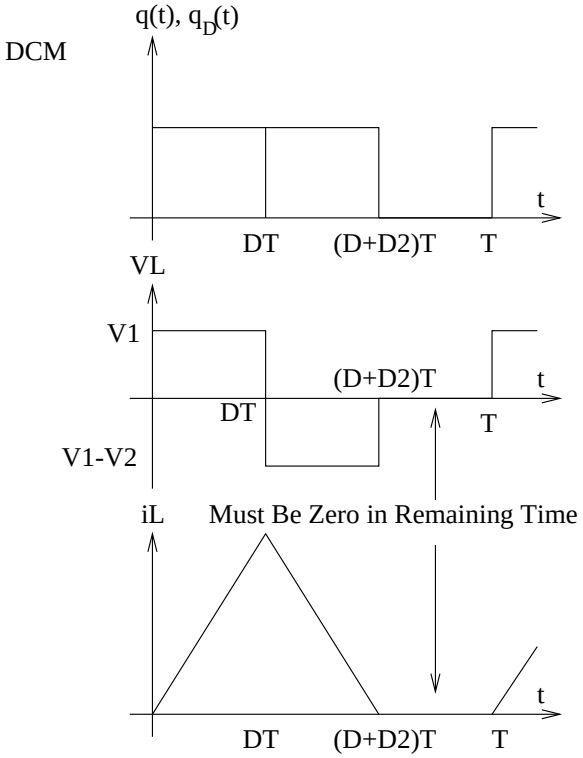

Figure 5.30: Different Operating Conditions

Voltage conversion ratio:

$$\begin{aligned} < V_L > &= 0 \; in \; P.S.S. \\ V_1 DT + (V_1 - V_2) D_2 T &= 0 \\ V_1(D + D_2) &= V_2 D_2 \\ \frac{V_2}{V_1} &= \frac{D + D_2}{D_2} \\ &= 1 + \frac{D}{D_2} \end{aligned} \tag{5.53}$$

where $D_2 < 1 - D$.

How does this compare to CCM? In CCM:

$$\frac{V_2}{V_1} = \frac{1}{1 - D}$$

$$\begin{aligned} &= \frac{1-D+D}{1-D} \\ &= 1+\frac{D}{1-D} \end{aligned} \tag{5.54}$$

Since $\frac{V_2}{V_1} = 1 + \frac{D}{D_2}$ and $D_2 < 1 - D$, $\frac{V_2}{V_1}$ is bigger in DCM.

Eliminating D_2 from equations, can be shown for boost:

$$\frac{V_2}{V_1} = \frac{1}{2} + \frac{1}{2}\sqrt{1+\frac{2D^2RT}{L}} \tag{5.55}$$

Therefore, conversion ratio depends on R, f_{sw}, L, ... unlike CCM. This makes control tricky, as all of our characteristics change for part of the load range.

How do we model DCM operation? Consider diode current (see Figure 5.31).

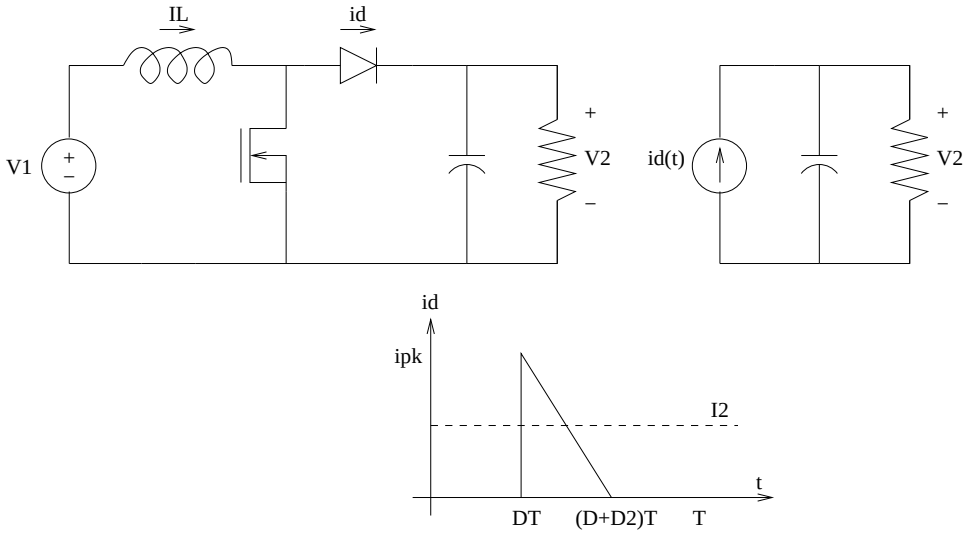

Figure 5.31: DCM Operation Model

$$\begin{aligned} i_{pk} &= \frac{V_1 DT}{L} \\ D_2 T &= \Delta t \end{aligned}$$

$$
\begin{aligned}
&= L\frac{\Delta i}{V} \\
&= L\frac{\frac{V_1 DT}{L}}{V_2 - V_1} \\
D_2 &= \frac{V_1 D}{V_2 - V_1} \qquad (5.56) \\
< i_{out} > &= < i_d > \\
&= \frac{1}{2}(D_2 T)(i_{pk})\frac{1}{T} \\
&= \frac{1}{2}(\frac{V_1}{V_2 - V_1}DT)(\frac{V_1 DT}{L})\frac{1}{T} \\
&= \frac{V_1^2 T D^2}{2(V_2 - V_1)} \qquad (5.57)
\end{aligned}
$$

Model as controlled current source as a function of D.

So DCM sometimes occurs under light load, as dictated by sizing of L.

- Sometimes we can not practically make L big enough.
- Must handle control (changes from CCM to DCM).
- Also, we get parasitic ringing in both switches (see Figure 5.32).

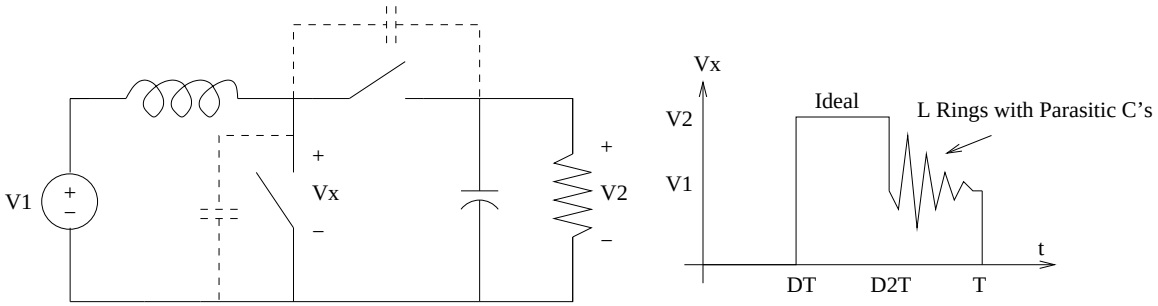

Figure 5.32: Parasitic Ringing

Sometimes people design to always be in DCM. Inductor size becomes very small and we can get fast $\frac{di}{dt}$ (see Figure 5.33).

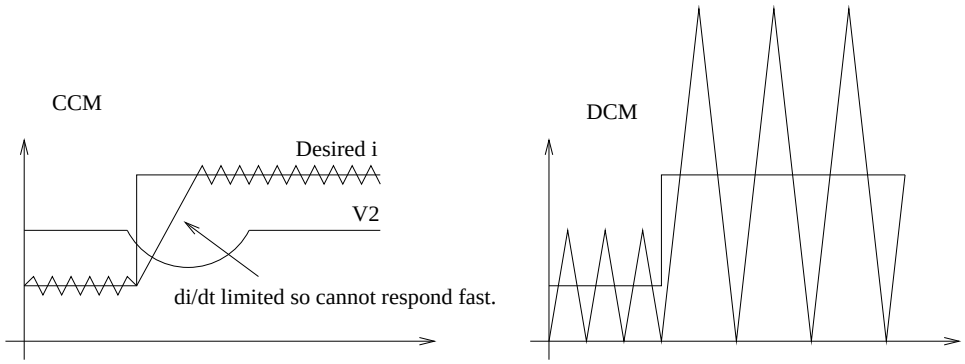

Figure 5.33: Design in DCM

In this case we get:

1. Very fast $\frac{di}{dt}$ capability.

2. Simple control model $i_{out} = f(D)$.

3. Small inductor size (E_L *minimized* @ $R_L = 1$)

But we must live with:

1. Parasitic ringing

2. High peak and RMS currents

3. Need additional filters

DCM is sometimes used when very fast response speed is needed (e.g. for voltage regulator modules in microprocessors), especially if means are available to cancel ripple (e.g. interleaving of multiple converters). In many other circumstances DCM is avoided, though one may have to operate in DCM under light-load conditions to keep component sizes acceptable.