**RF I IF**

# RF Power Amplifiers

**May 7, 2003**

**ANALOG DEVICES**

# Outline

◆ **PA Introduction**
- **Power transfer characteristics**
- **Intrinsic PA metrics**
- **Linear and Non-linear amplifiers**
- **PA Architectures**

◆ **Single-Stage Linear PA**
- **Load-line theory**
- **Transistors size**
- **Input and Output Matching**
- **So why is this so hard?**

◆ **High-efficiency PAs**
- **Class A, AB, B and C amplifiers**

# Outline (cont.)

◆ **Real-World Design Example**

- **Selecting architecture, number of stages**
- **Designing stages**
- **Tuning: inter-stage match and output**

◆ **System specifications**

- **Ruggedness: load mis-match and VSWR**
- **Linearity: spectral mask (ACPR), switching transients**
- **Noise in receive band**

◆ **Power Control**
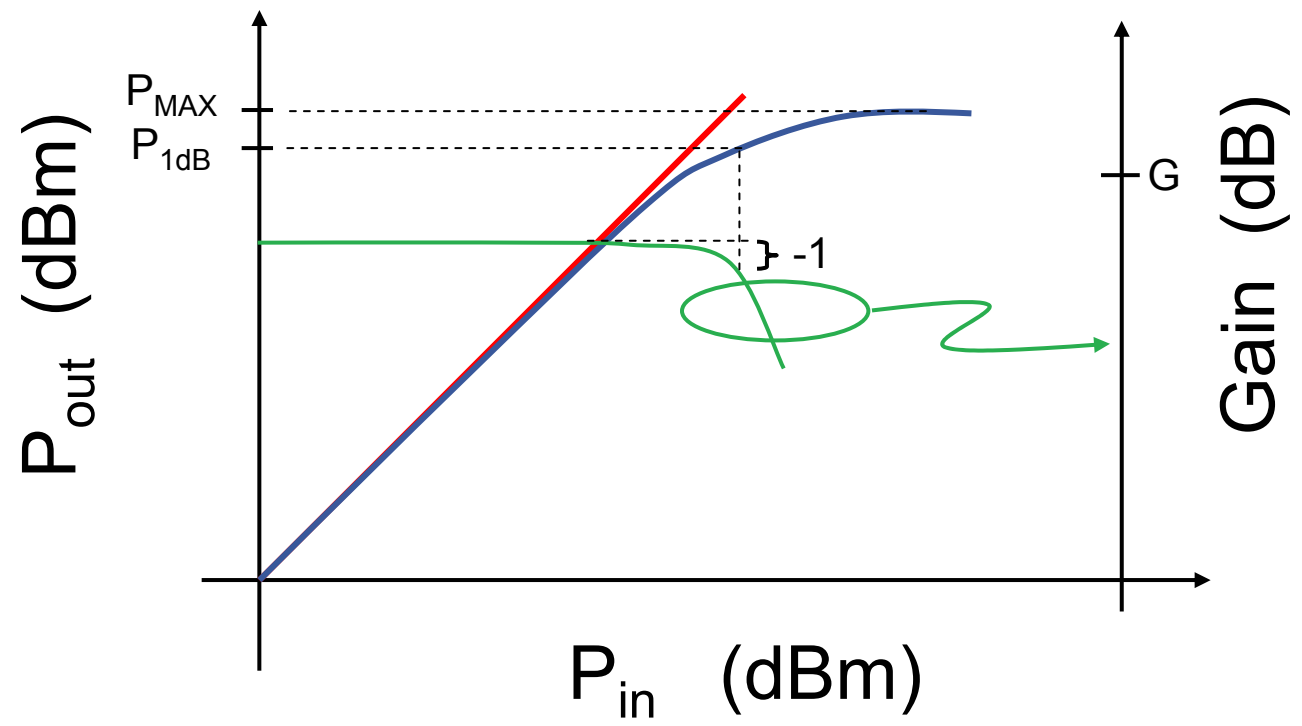
3

# PA Transfer characteristics

## Defining linearity:



linear

non-linear (actual)

$P_{out} = P_{in} + G$

$P_{out}$ (dBm)

$P_{in}$ (dBm)

G

0

1
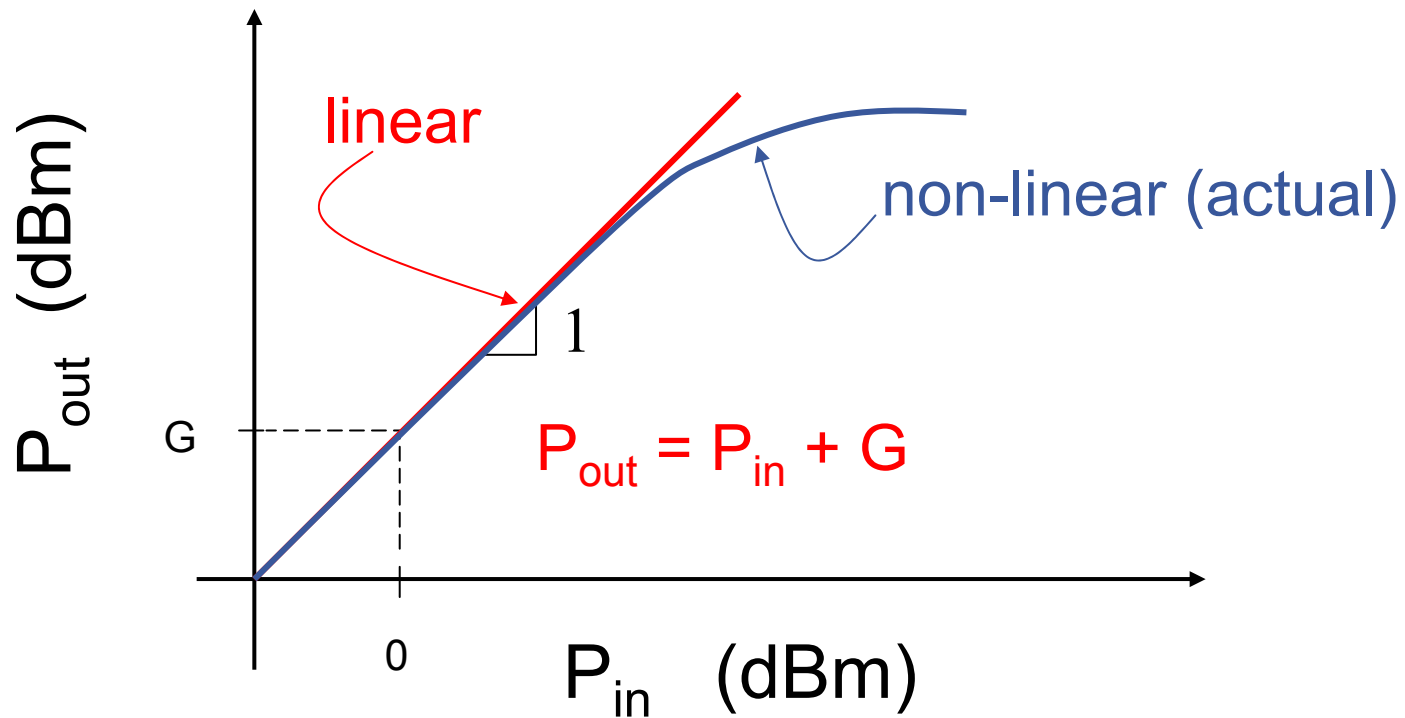
# PA Transfer characteristics

## Defining linearity:

# PA Introduction: Intrinsic PA Metrics

◆ **$P_{1dB}$: Output power at which linear gain has compressed by 1dB (measure of linear power handling)**

◆ **$P_{MAX}$: Maximum output power (saturated power)**

◆ **Gain: Generally taken to mean transducer gain**

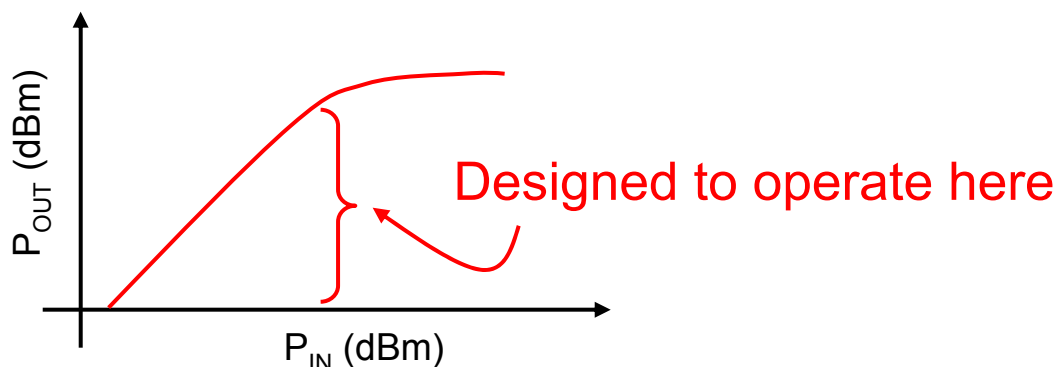$$\frac{\text{Power delivered to load}}{\text{Power available from source}}$$

◆ **PAE: Power-added Efficiency**

$$\frac{\text{Power to load} - \text{Power from source}}{\text{Power from supply}}$$

# Linear and Non-linear PAs

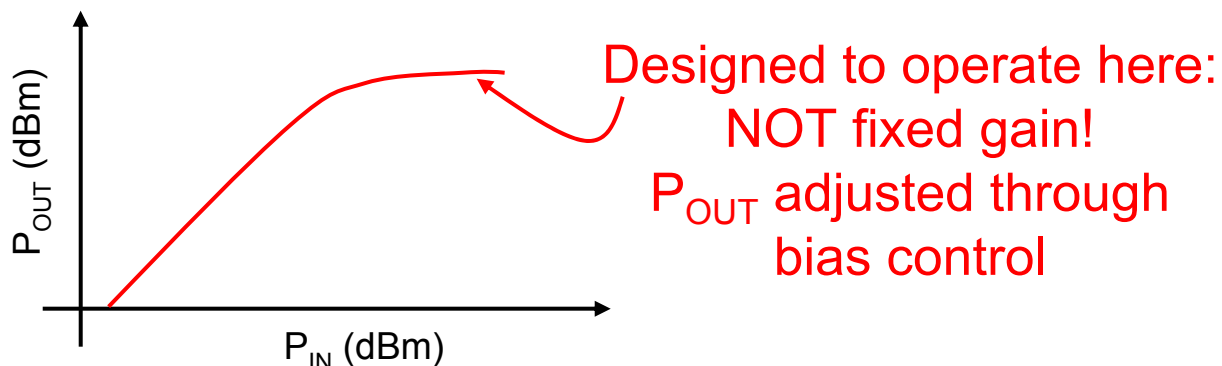◆ **"Linear PA" generally refers to a PA which operates at constant gain, needs to preserve amplitude information**



◆ **Not necessarily class A (will discuss later …) Peak efficiencies often only 40 to 45 %**

◆ **Useful for modulation schemes with amplitude modulation (QPSK, 8-PSK, QAM)**
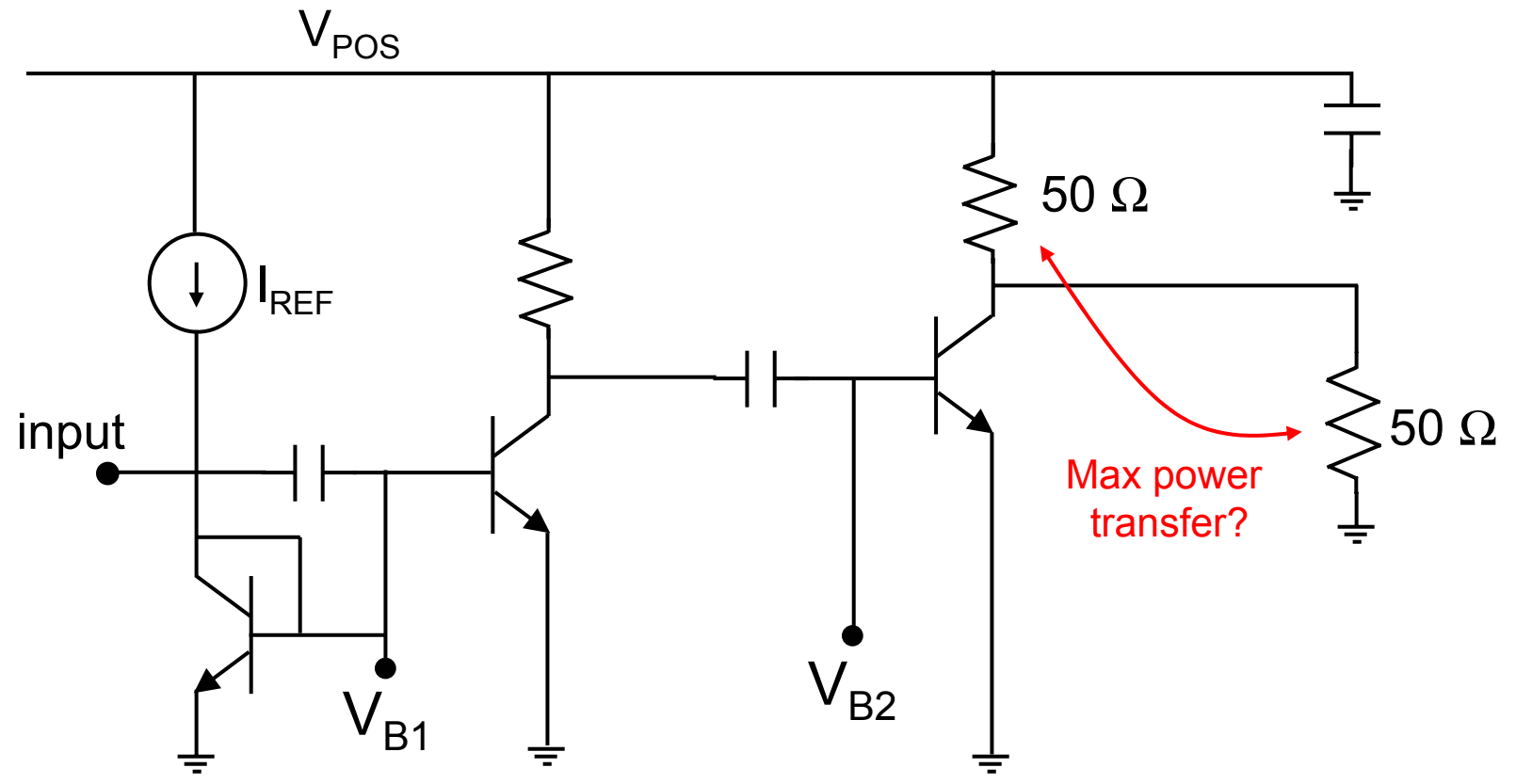
ANALOG
DEVICES

# Linear and Non-linear PAs

◆ **"Non-linear PA" generally refers to a PA designed to operate with constant $P_{IN}$, output power varies by changing gain**



Plot of $P_{OUT}$ (dBm) versus $P_{IN}$ (dBm) with a red curve that rises and saturates.

Designed to operate here:
NOT fixed gain!
$P_{OUT}$ adjusted through
bias control

◆ **Operation in saturated mode leads to high peak efficiencies > 50%; "backed-off" efficiencies drop quickly**
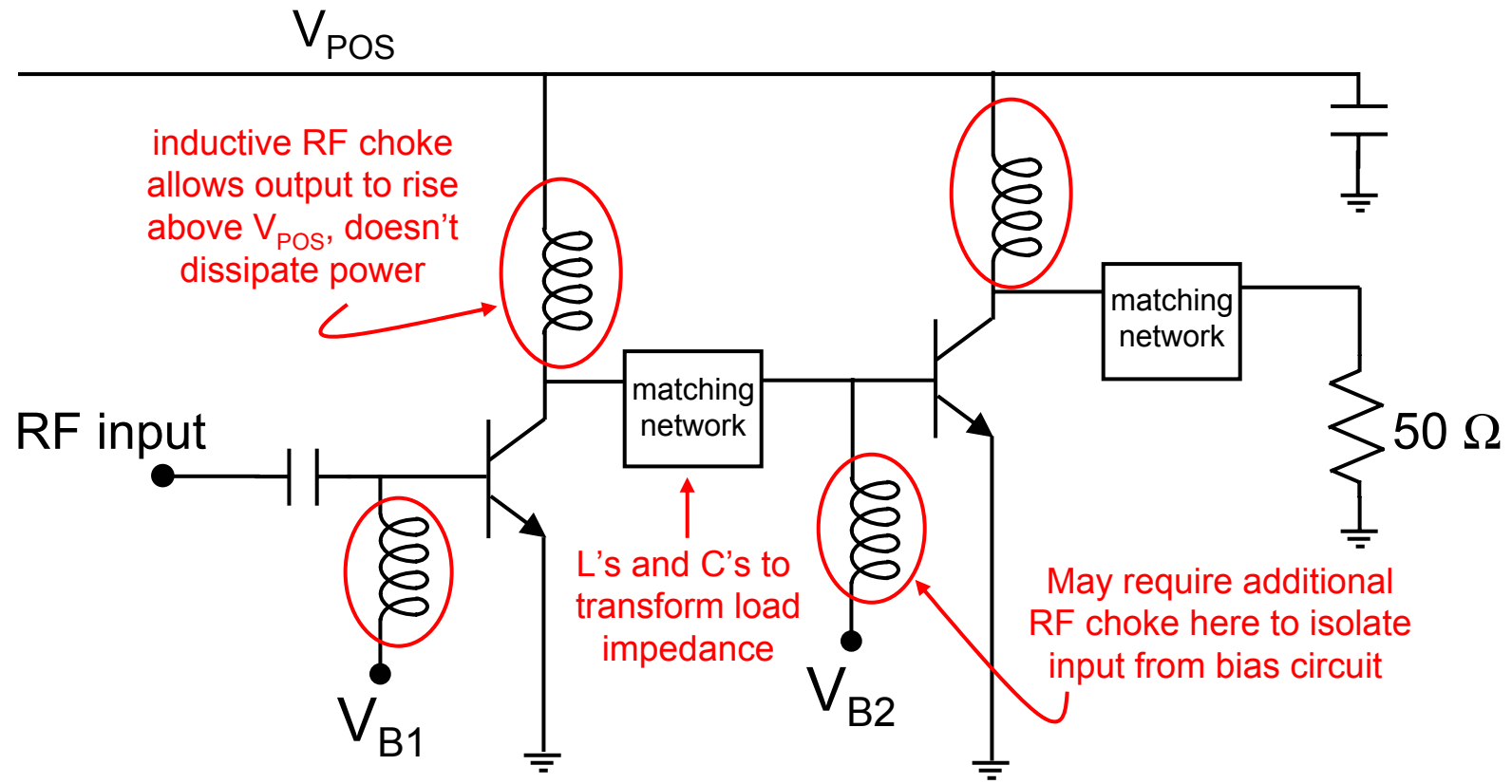
◆ **Useful for constant-envelope modulation schemes (GMSK)**
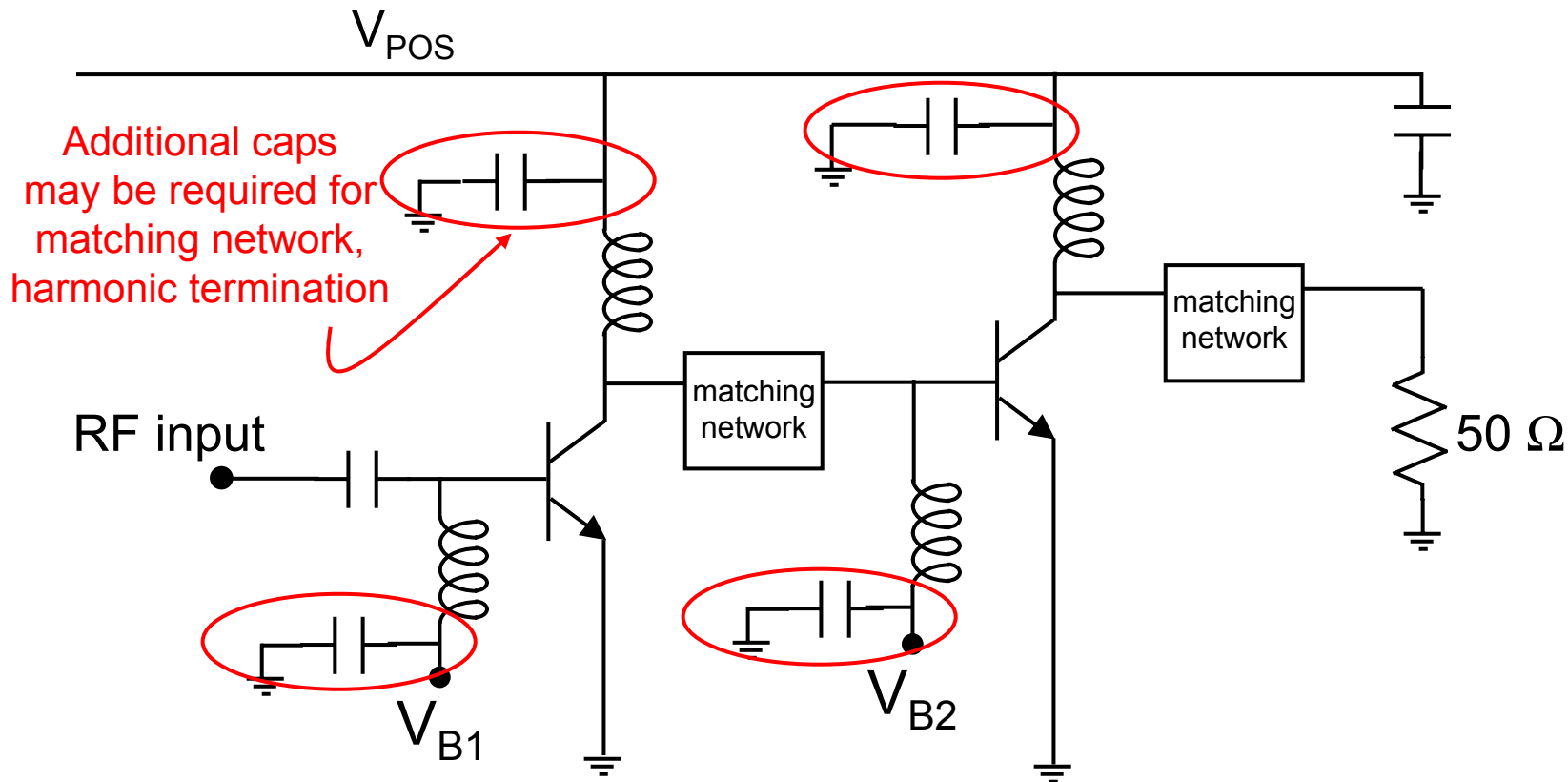
8

# PA Architectures

## Typical 2-stage (6.012) design



Max power transfer?

ANALOG DEVICES

# PA Architectures

## Typical 2-stage RF PA design



$V_{POS}$

inductive RF choke allows output to rise above $V_{POS}$, doesn't dissipate power

matching network

matching network

RF input

50 Ω

L's and C's to transform load impedance

$V_{B1}$

$V_{B2}$

May require additional RF choke here to isolate input from bias circuit

# PA Architectures

## Typical 2-stage RF PA design



$V_{POS}$

Additional caps may be required for matching network, harmonic termination

RF input

matching network

matching network

50 $\Omega$

$V_{B1}$

$V_{B2}$
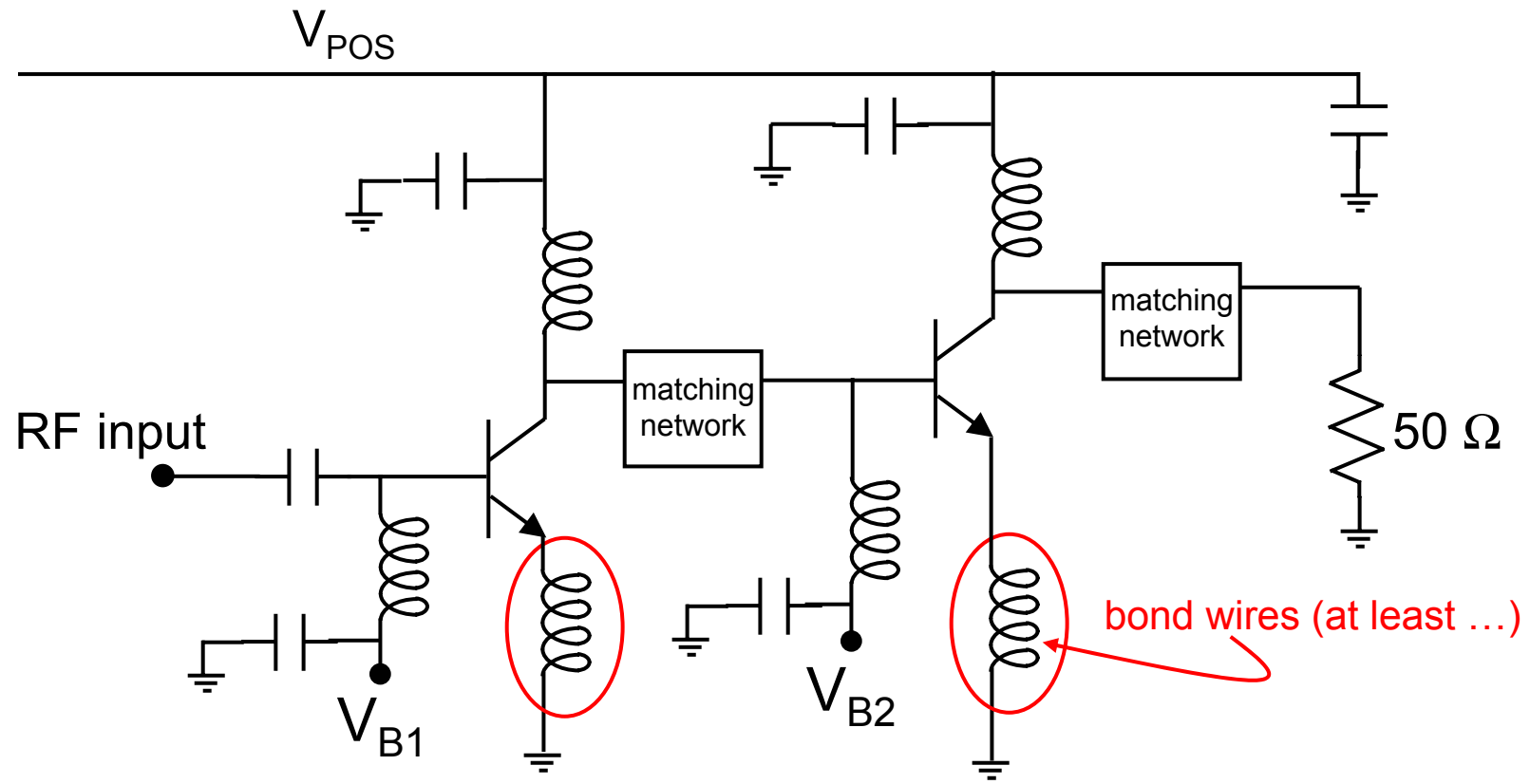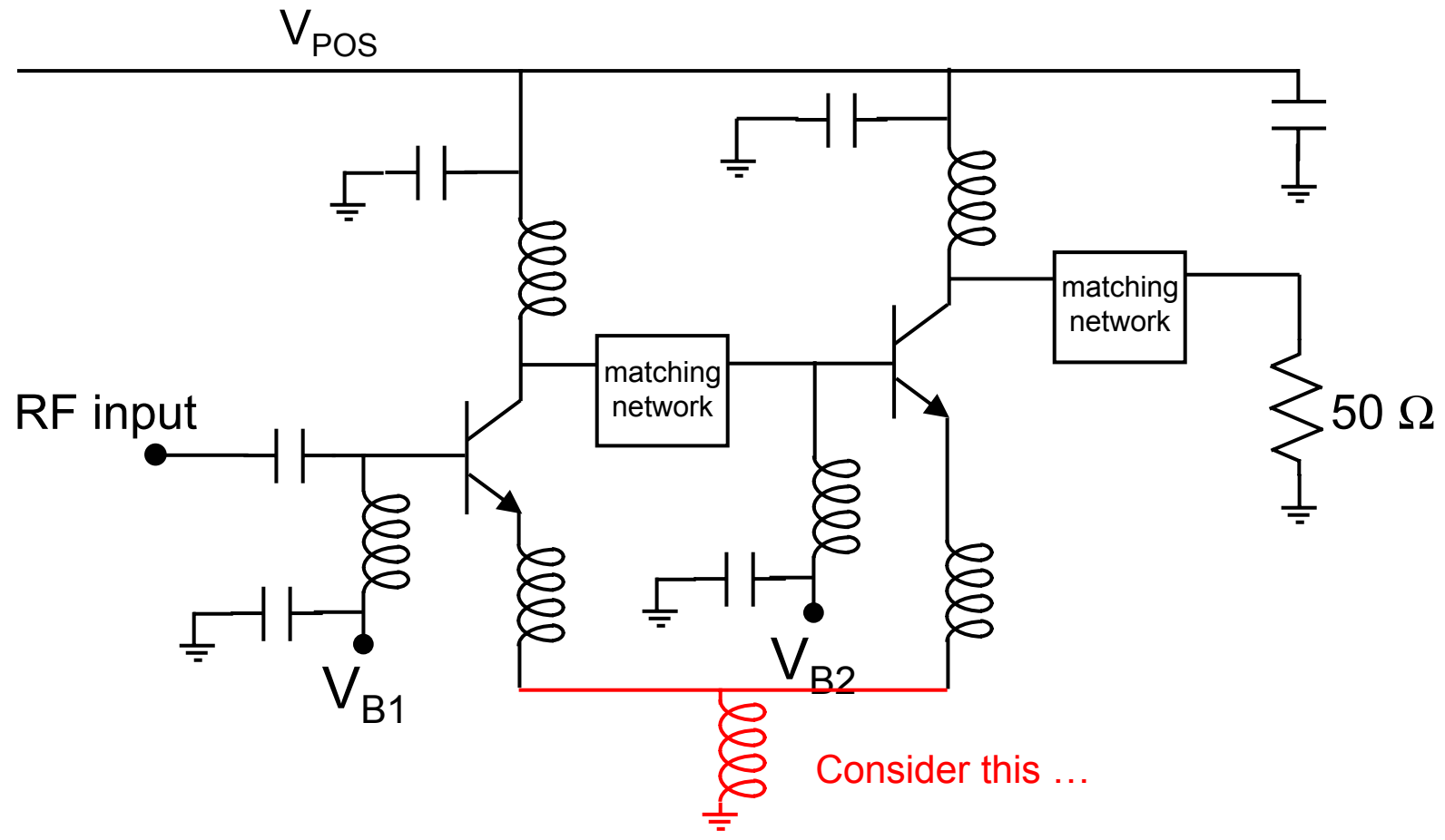
# PA Architectures

## Typical 2-stage RF PA design

# PA Architectures
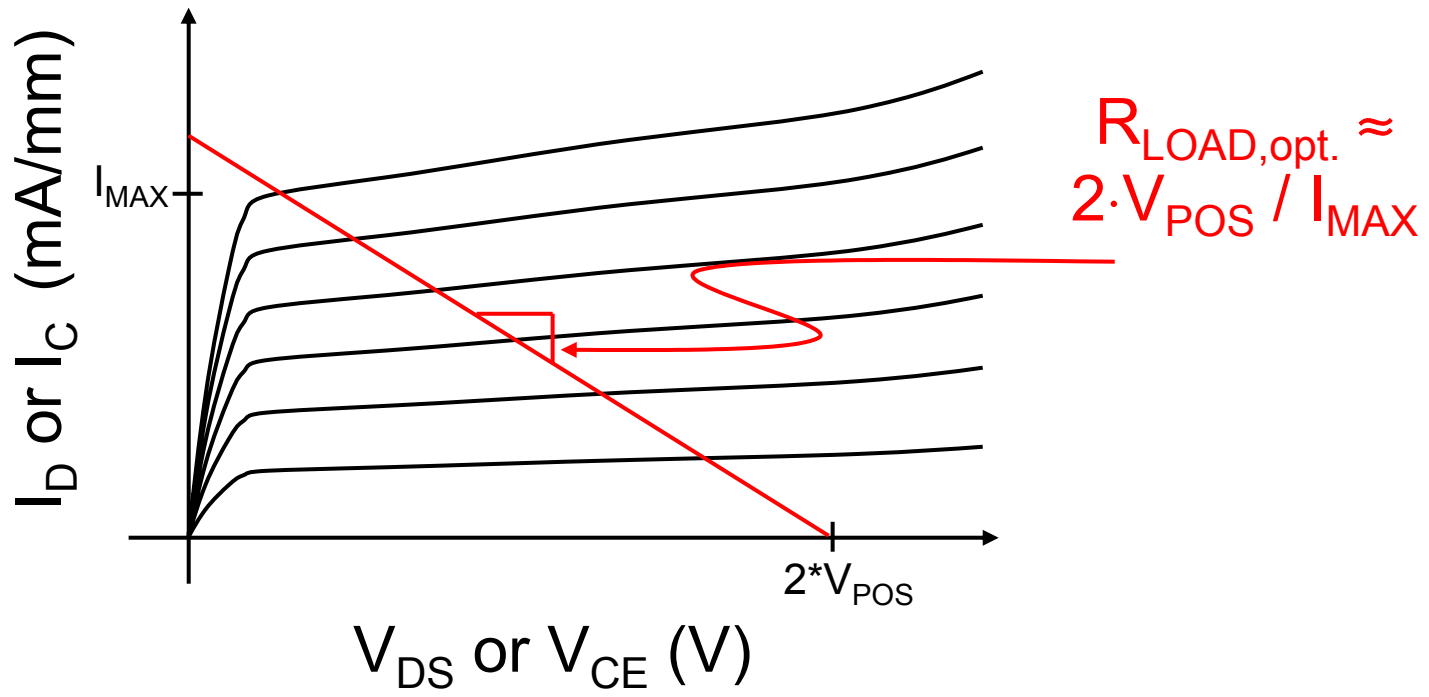
## Typical 2-stage RF PA design

# PA Architectures

- ◆ **"Gain stage" is one transistor with passive elements**
- ◆ **"Active" components often limited to 2 or 3 transistors (gain stages) in signal path**
- ◆ **Transistor design very important!**
  - ● **Many parallel transistors – often look like mini-circuits themselves**
- ◆ **Passive components just as important as transistors!**
  - ● **Circuits must be tunable to account for uncertainties in determining values *a priori* (i.e. simulations stink – especially large-signal, RF simulations)**
  - ● **Q and parasitic elements of passives important**

# Single-Stage Linear PA

◆ **Load-line theory: the maximum power that a given transistor can deliver is determined by the power supply voltage and the maximum current of the transistor**
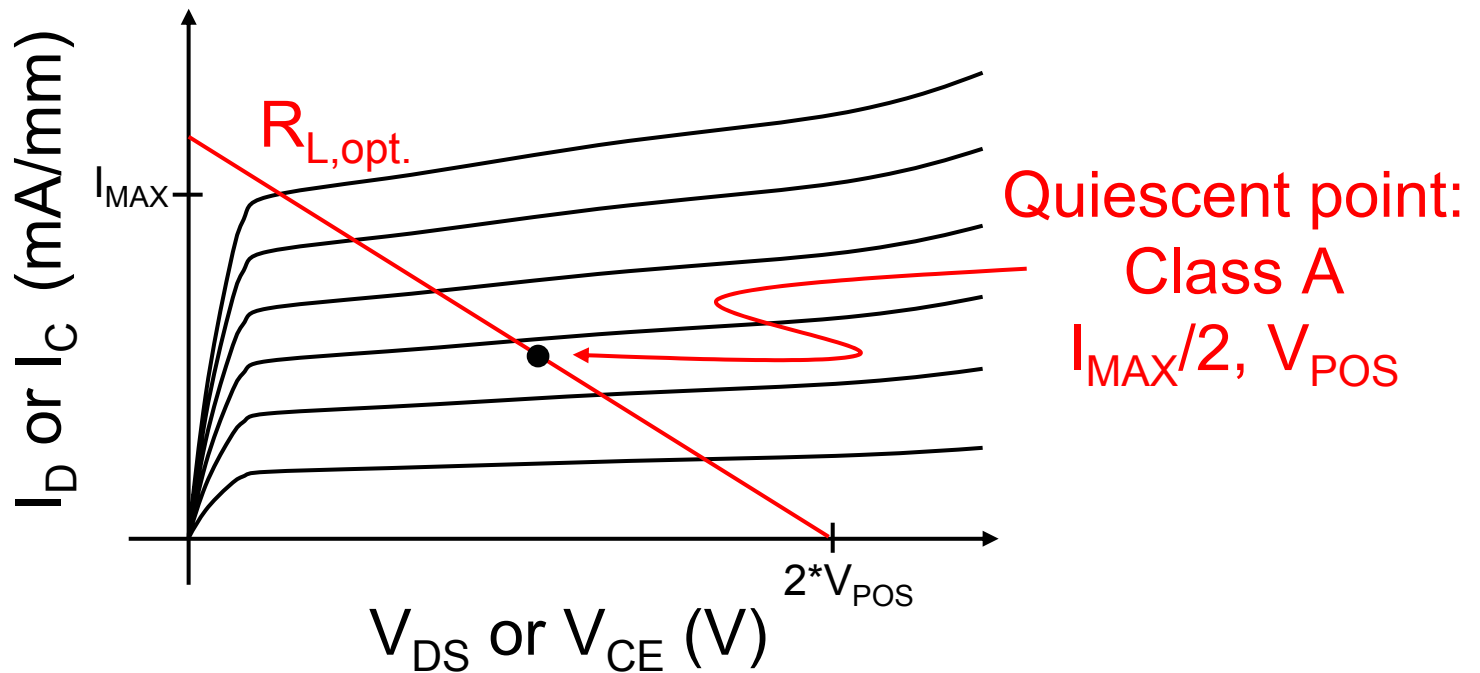


$R_{LOAD,opt.} \approx 2 \cdot V_{POS} / I_{MAX}$

$I_D$ or $I_C$ (mA/mm)

$I_{MAX}$

$V_{DS}$ or $V_{CE}$ (V)

$2 * V_{POS}$

**ANALOG DEVICES**

# Single-Stage Linear PA

◆ **Transistor size chosen to deliver required output power**

$$P_{OUT} \approx I_{MAX} \cdot V_{POS} / 4$$



$R_{L,opt.}$

$I_{MAX}$

Quiescent point:
Class A
$I_{MAX}/2$, $V_{POS}$

$I_D$ or $I_C$ (mA/mm)

$V_{DS}$ or $V_{CE}$ (V)

$2*V_{POS}$

# Single-Stage, Linear PA

◆ **Design output match to transform 50Ω load to $R_{L,opt}$ at transistor output; then design input match for gain (complex conjugate)**
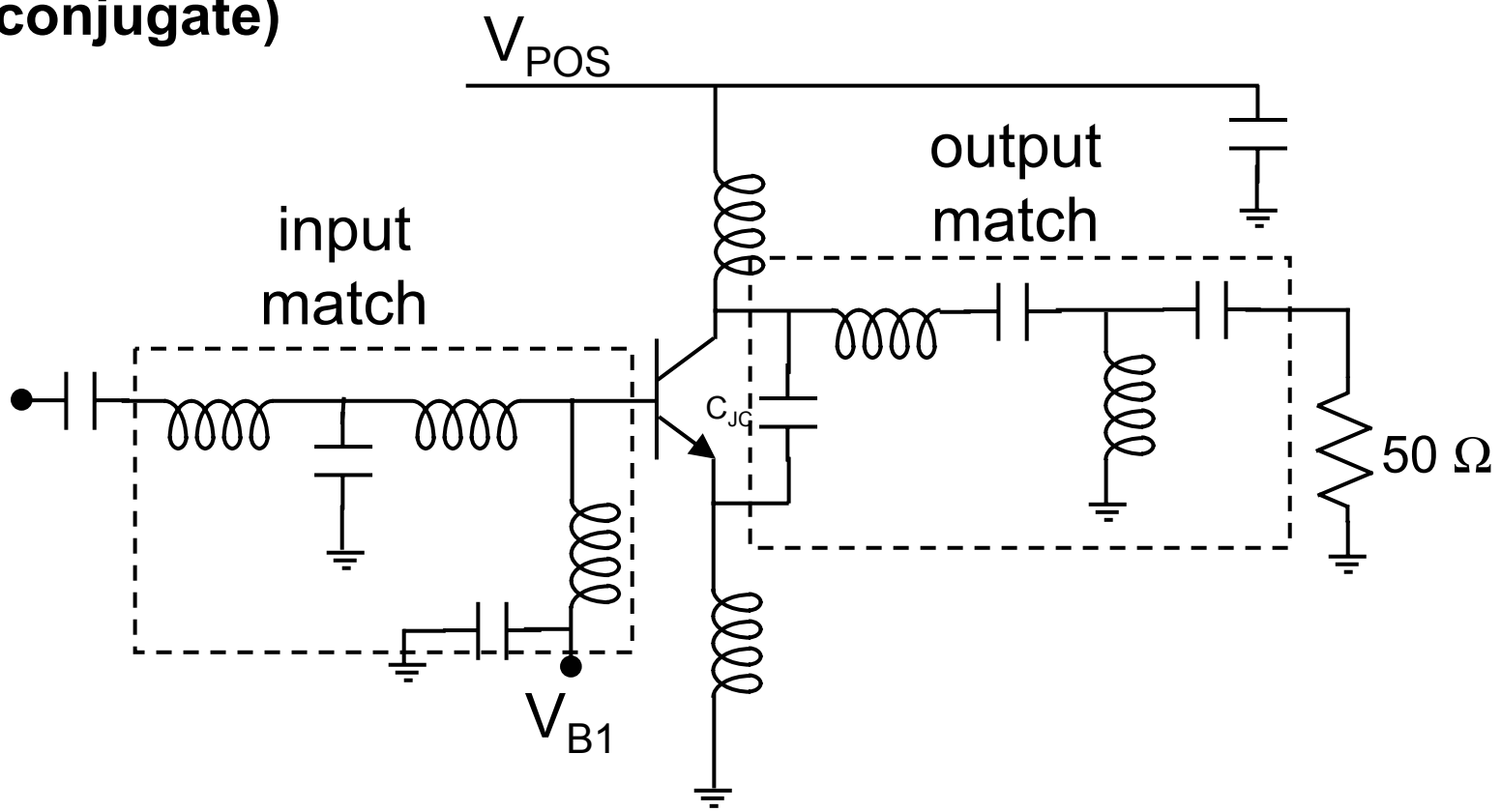
# Seems simple, so why is this so hard?

- ◆ **Determining $I_{MAX}$ is not so easy**
  - ● **For BJTs, one reference suggested that "the best way of estimating its value is to build an optimized class A amplifier and observe the dc supply current."[1]**
  - ● **Somewhat easier for depletion-mode GaAs FETs – $I_{MAX}$ often corresponds to $V_{GS}$ = 0V**
  - ● **Values don't scale linearly with transistor size**
- ◆ **Optimal load resistance only a theoretical number**
  - ● **Transmission line effects, parasitic L's and C's significant at RF**
  - ● **Common practice is to vary the load of an actual transistor to determine the peak output power: the load-pull measurement**

    **(Noticing a distinct pattern of "empirical" design emerging?)**

[1] RF Power Amplifiers for Wireless Communications, Steve Cripps, Artech House, Boston, 1999.

**ANALOG DEVICES**

# Seems simple, so why is this so hard?

◆ **Now consider the problem for multiple stages … double the trouble**

  ● **Typical single-stage gain only 10 – 15 dB**

  ● **Inter-stage match now required to match input impedance of 2$^{nd}$ stage to desired output impedance of 1$^{st}$ stage.**

◆ **Problems with matching circuits:**

  ● **Large matching ratios $\rightarrow$ high Q circuits for simple L matches**

  ● **Multi-segment matches use valuable real estate, add cost**

◆ **Transistor itself maters – a lot!**

  ● **Many parallel transistor**

  ● **Ballasting, balancing and layout extremely important**

**ANALOG
DEVICES**

# High-efficiency PAs

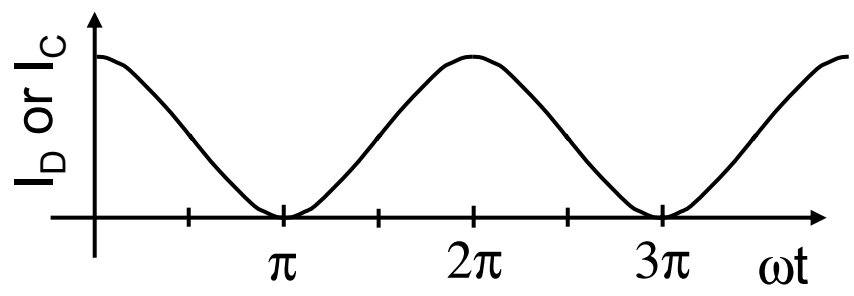◆ **Input signal swing turns on transistor – conduction for only part of sinusoidal period**
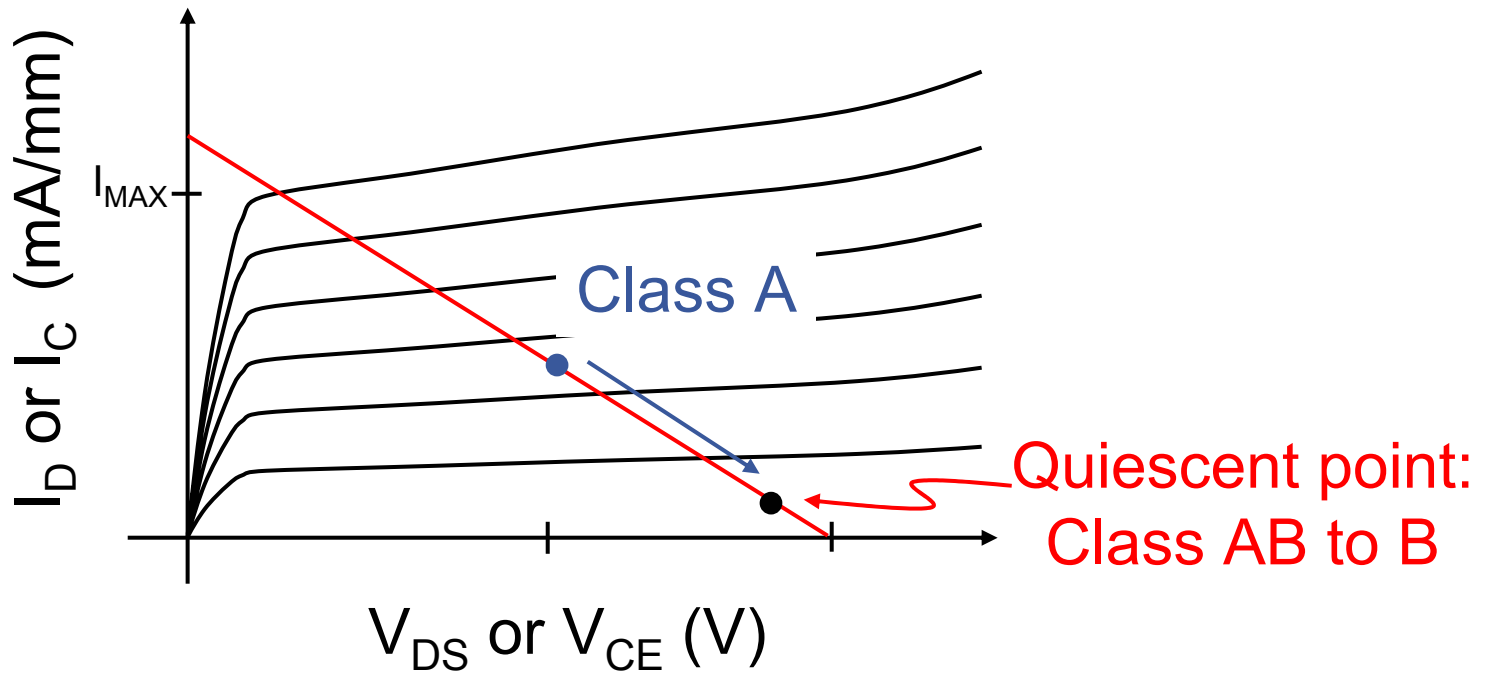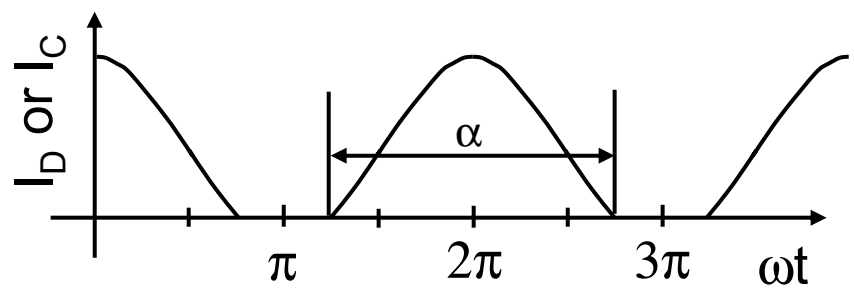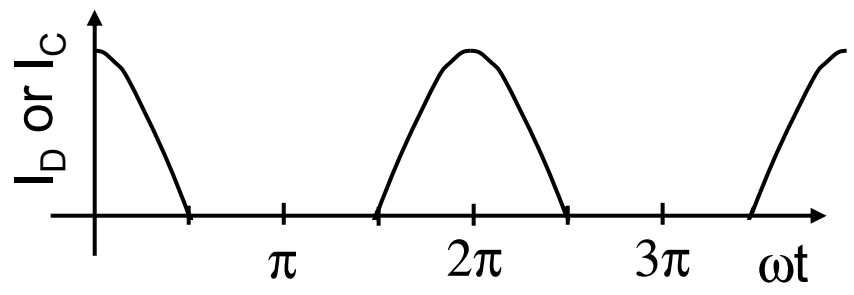
# High-Efficiency PAs

Conduction Angle:

Class A:



$\alpha = 2\pi$

Class AB:



$\pi < \alpha < 2\pi$

Class B:



$\alpha = \pi$

Class C: $\alpha < \pi$

# High-Efficiency PAs

◆ **Assume output match will filter out non-linearities caused by discontinuous conduction:**

input
match

output
match

$V_{B1}$

50 Ω

50Ω transformed
to $R_{L,opt}$:
All harmonics
filtered out
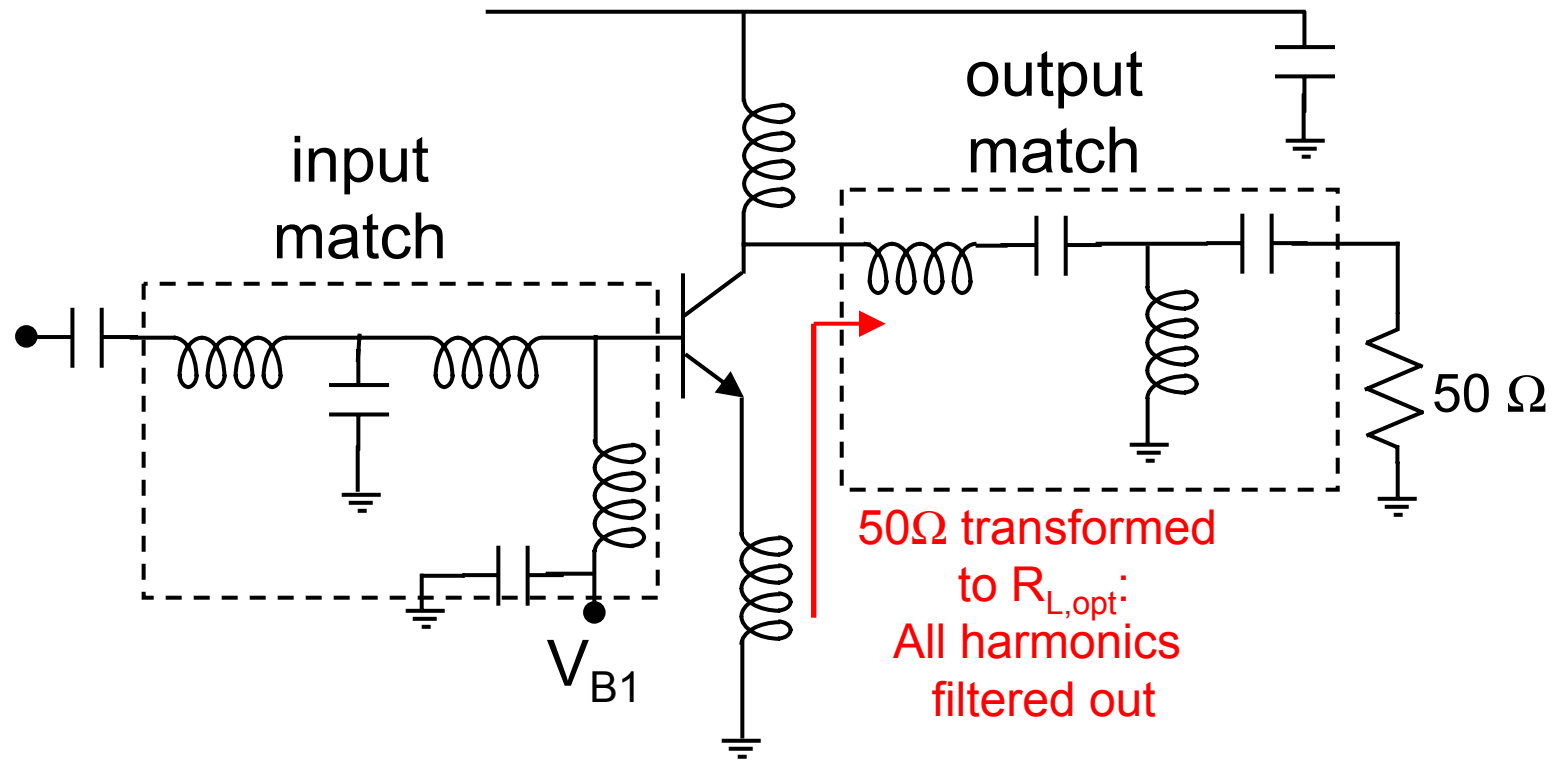
# High-Efficiency PAs

◆ **If all harmonics filtered out, then voltage output at load is a pure sinusoid, despite discontinuous conduction**
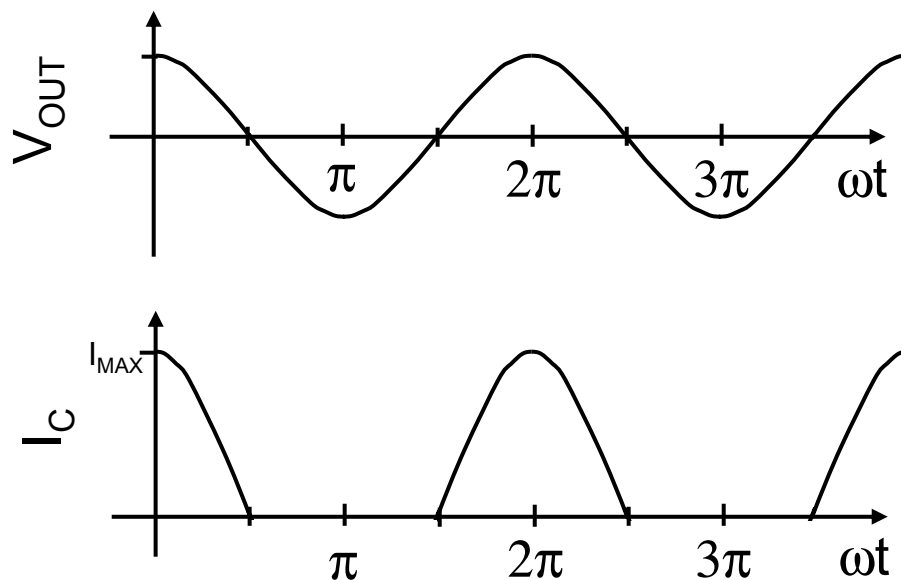


◆ **Energy stored in reactive elements delivers current to the load during transistor off-portion of cycle**
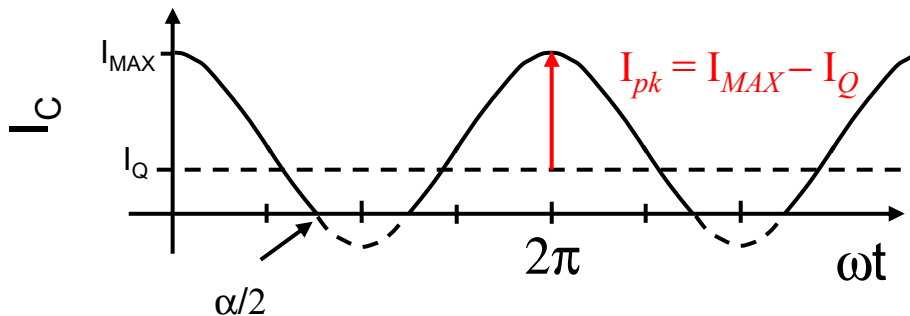
# High-Efficiency PAs

◆ **Now consider peak efficiencies**

**Calculate fundamental component of current[*]**

$$I_{dc} = (1/2\pi)\int_{-\alpha/2}^{\alpha/2} I_Q + I_{pk}\cos(\omega t)\,d\omega t$$

$$I_n = (1/\pi)\int_{-\alpha/2}^{\alpha/2} I_{pk}\cos(\omega t)\cos(n\omega t)\,d\omega t$$



$I_{pk} = I_{MAX} - I_Q$

[*] There are many texts which cover reduced-conduction angle calculations. See for example *Principles Of Power Electronics,* Kassakian, Schelcht and Verghese, Ch. 3.

24

# High-Efficiency PAs

**From phasor plot:** $\cos(\alpha/2) = -\, I_Q / I_{pk} = -\, I_Q / (I_{MAX} - I_Q)$

**Put it all together and do the math, you get:**

$$I_{dc} = \frac{I_{MAX}}{2\pi} \, \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)}$$

$$I_{1,0\text{-}p} = \frac{I_{MAX}}{2\pi} \, \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)}$$

**Assume V$_{OUT}$ the same for all classes:**

$$V_{1,0\text{-}p} = V_{POS}$$

ANALOG
DEVICES

# High-Efficiency PAs

◆ **Summary of PA "ideal" peak efficiencies**

Class A: $\dfrac{P_1}{P_{dc}} = \dfrac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{(I_{MAX}/2) \cdot V_{POS}} = 50\ \%$

Class B: $\dfrac{P_1}{P_{dc}} = \dfrac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{(I_{MAX}/\pi) \cdot V_{POS}} = 78\ \%$
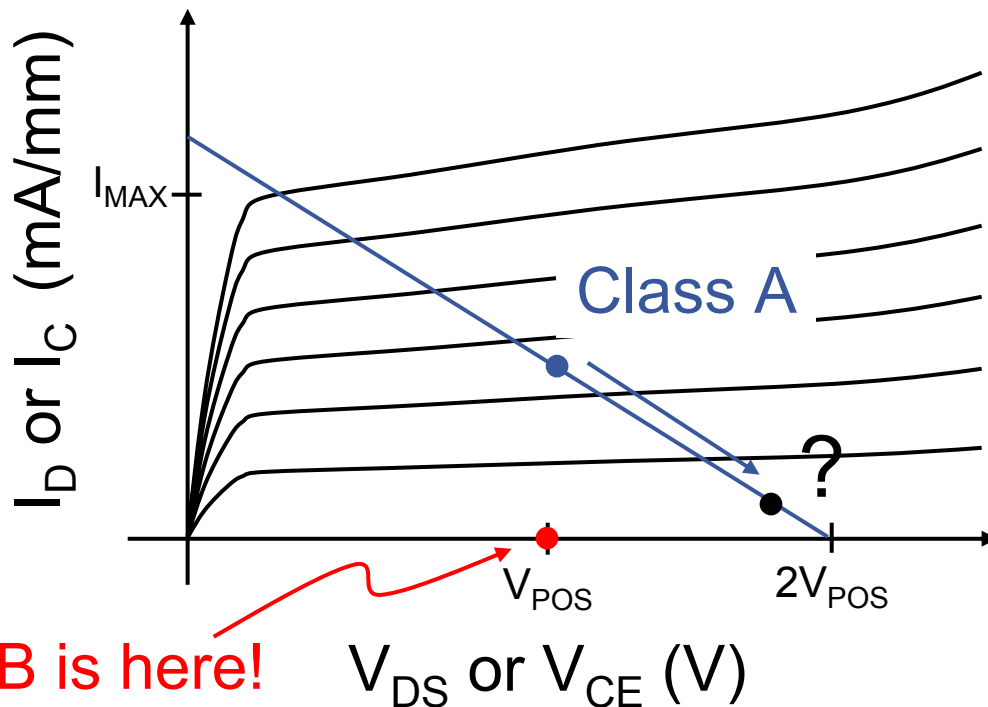
Class C: Ideally can go to 100%, but $P_1$ drops steadily beyond $\alpha=\pi$, goes to 0 at 100%!

# High-Efficiency PAs

- ◆ **What happened to our load line?**
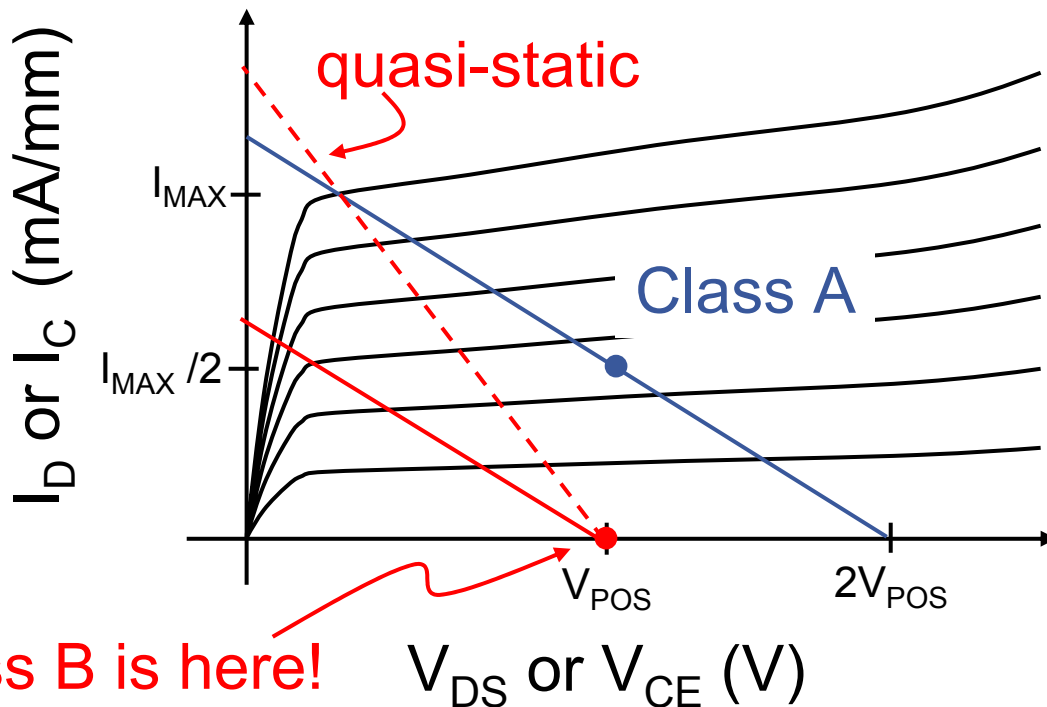  - ● **For class B fundamental $R_{L,opt} = V_{POS}/(I_{MAX}/2)$ – Didn't change**

# High-Efficiency PAs

◆ **What happened to our load line?**

  ● **For class B fundamental $R_{L,opt} = V_{POS}/(I_{MAX}/2)$ – Didn't change**



quasi-static

Class A

Class B is here!

$I_{MAX}$

$I_{MAX}/2$

$I_D$ or $I_C$ (mA/mm)

$V_{POS}$

$2V_{POS}$

$V_{DS}$ or $V_{CE}$ (V)

In quasi-static picture, resistance presented to transistor output cut in half.  But average resistance is the same for class A
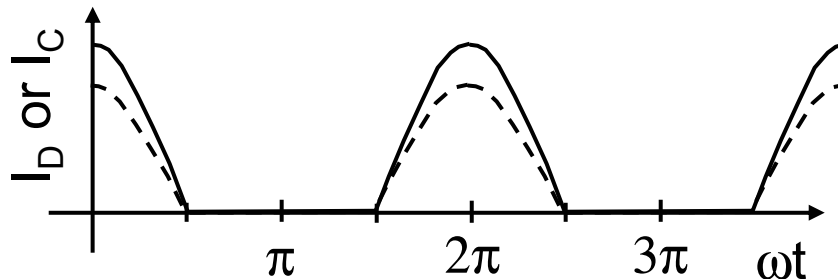
28

# High-Efficiency PAs

◆ **Now consider "linearity"**

● **Clearly the current waveforms are far from linear**

**BUT …**

● **Overall $P_{OUT}$ vs. $P_{IN}$ transfer function can still be quite linear, especially for true Class B where output current waveform is symmetrical with respect to input waveform**



Because conduction angle is constant,
$P_{OUT}$ changes proportional to $P_{IN}$

# Real-World Design Example

◆ **IDEAL: Design each stage independently**

- **Determine required gain – number of stages**
- **Determine $P_{OUT}$ for each stage**
- **Determine $R_{L,opt}$ for each stage**
- **Determine input impedance for each stage**
- **Design matching networks for inter-stage, load and input**

◆ **REALITY:**

- **$I_{MAX}$ doesn't scale nicely with transistor size. Without good $I_{MAX}$ numbers, can't determine $R_{L,opt}$. Need to do load-pull.**
- **Even load pull measurements have limited accuracy for very large transistors**
- **Designs are very empirically driven!**

# Real-World Design Example

GSM 900 MHz, GaAs HBT PA Design

◆ $P_{OUT}$ = 33 dBm (linear) = 2 W

$V_{CC}$ = 3.5V

$R_{LOAD} = V_{CC}^2 / 2*P_{OUT}$ = 3 $\Omega$

$I_{MAX} = 2*V_{CC} /R_{LOAD}$ = 2.33 A

(Note: expect saturated power to be ~ 35 dBm)

◆ Input power: constant-envelope +5 dBm

◆ Gain =  $P_{OUT} - P_{IN}$  = 27 dB.

◆ Expect roughly 10 dB per stage

3 STAGE DESIGN

# Real-World Design Example

- **Stage 1: Gain = 10 dB $\rightarrow$ $P_{OUT}$ = 15 dBm**
  - $R_{L1} = V_{CC}^2 / 2 \cdot P_{OUT} = 194\ \Omega$
  - $I_{MAX} = 2 \cdot V_{CC} / R_{LOAD} = 36$ mA
  - Chose class A: $I_{DC} = I_{MAX}/2 = 18$ mA
    (18 mA insignificant compared to 2.33 A)
- **Stage 2: Gain = 10 dB $\rightarrow$ $P_{OUT}$ = 25 dBm**
  - $R_{L2} = 19.4\ \Omega$
  - $I_{MAX} = 360$ mA
  - Still probably class A (maybe AB): $I_{DC} = I_{MAX}/2 = 180$ mA
- **Stage 3: Gain = 7 dB $\rightarrow$ $P_{OUT}$ = 33 dBm**
  - $R_{L2} = 3\ \Omega$, $I_{MAX} = 2.33$ A
  - Class B: $I_{DC} = I_{MAX}/\pi = 742$ mA

# Real-World Design Example

## A note on "Gain"

◆ **Taking a very simplistic view of common emitter stages:**

- $g_{m1} = I_C / V_{Th} = 18\ mA / 0.025\ V = 0.696\ S$

- $g_{m1}R_{L1} = 0.696 \cdot 194 = 135 \rightarrow$ **NOT 10 dB!**

**BUT …**

- $r_{e1} = 1/g_{m1} = 1.44\ \Omega$

- $r_{e2} = 1/g_{m2} = 0.144\ \Omega$

- $r_{e3} = 1/g_{m3} = 0.035\ \Omega$

1. Remember it's power gain, not voltage gain.  Can lose voltage at input match.

2. It's pretty tough not to get significant degeneration!

# Real-World Design Example
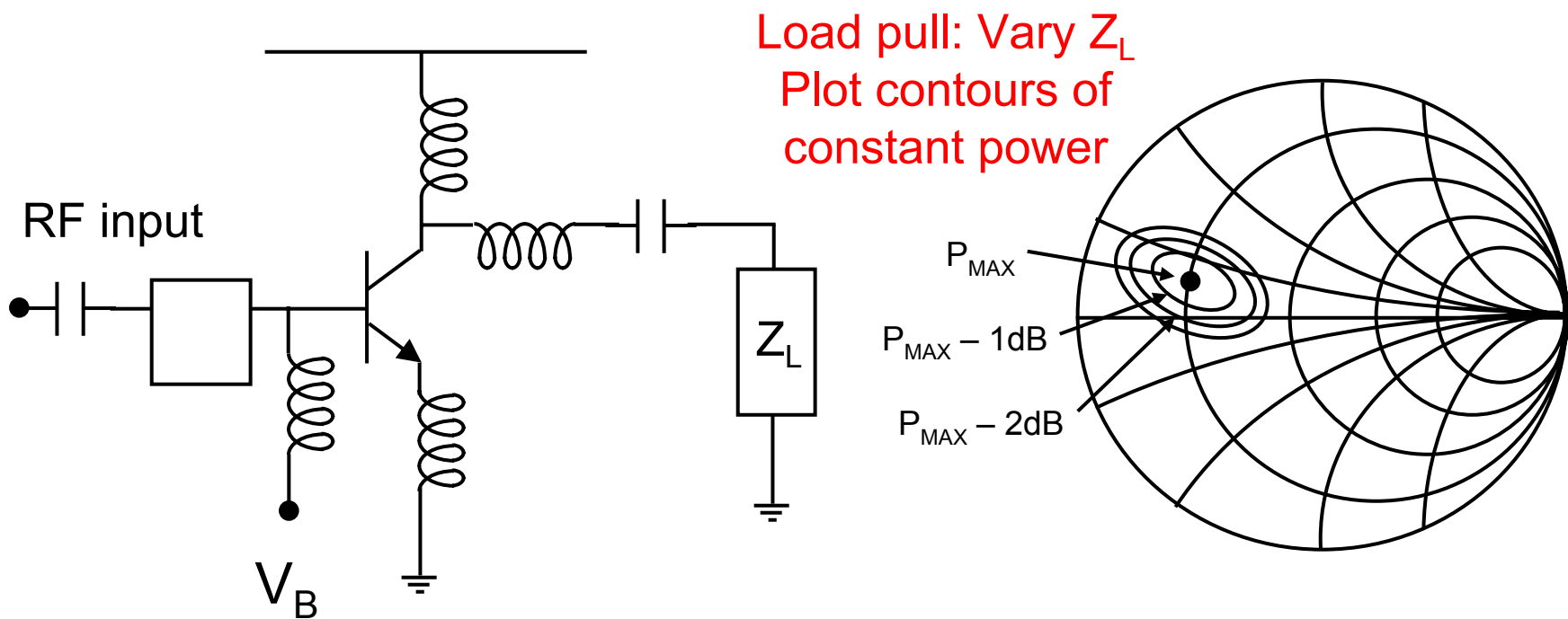
---

◆ **Efficiency calculations:**

- **$I_{DC1}$ = 18 mA, $I_{DC2}$ = 180 mA, $I_{DC3}$ = 742 mA**
- **Total DC Current: 940 mA**

$$\frac{P_1}{P_{dc}} = \frac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{I_{DC} \cdot V_{POS}} = 62\,\%$$

- **Realistically may get as high as 55%**

---

# Real-World Design Example: Load-Pull

◆ **After initial "guesses" at transistor sizes, load-pull to determine actual target load for matching circuits**

Load pull: Vary $Z_L$
Plot contours of
constant power

RF input

$Z_L$

$V_B$

$P_{MAX}$

$P_{MAX} - 1dB$

$P_{MAX} - 2dB$

ANALOG
DEVICES

# Real-World Design Example: Load-pull

## Notes on load-pulling:

◆ **Most accurate on probe station, but insertion loss of probes prevents it from being useful for large transistors**

**("Insertion loss" is RF code word for resistance)**

◆ **Bonded devices on evaluation board must be carefully de-embedded**

◆ **Even using electronic tuners, accuracy is poor for very large transistor (i.e. for loads in the 2 – 5 $\Omega$ range)**
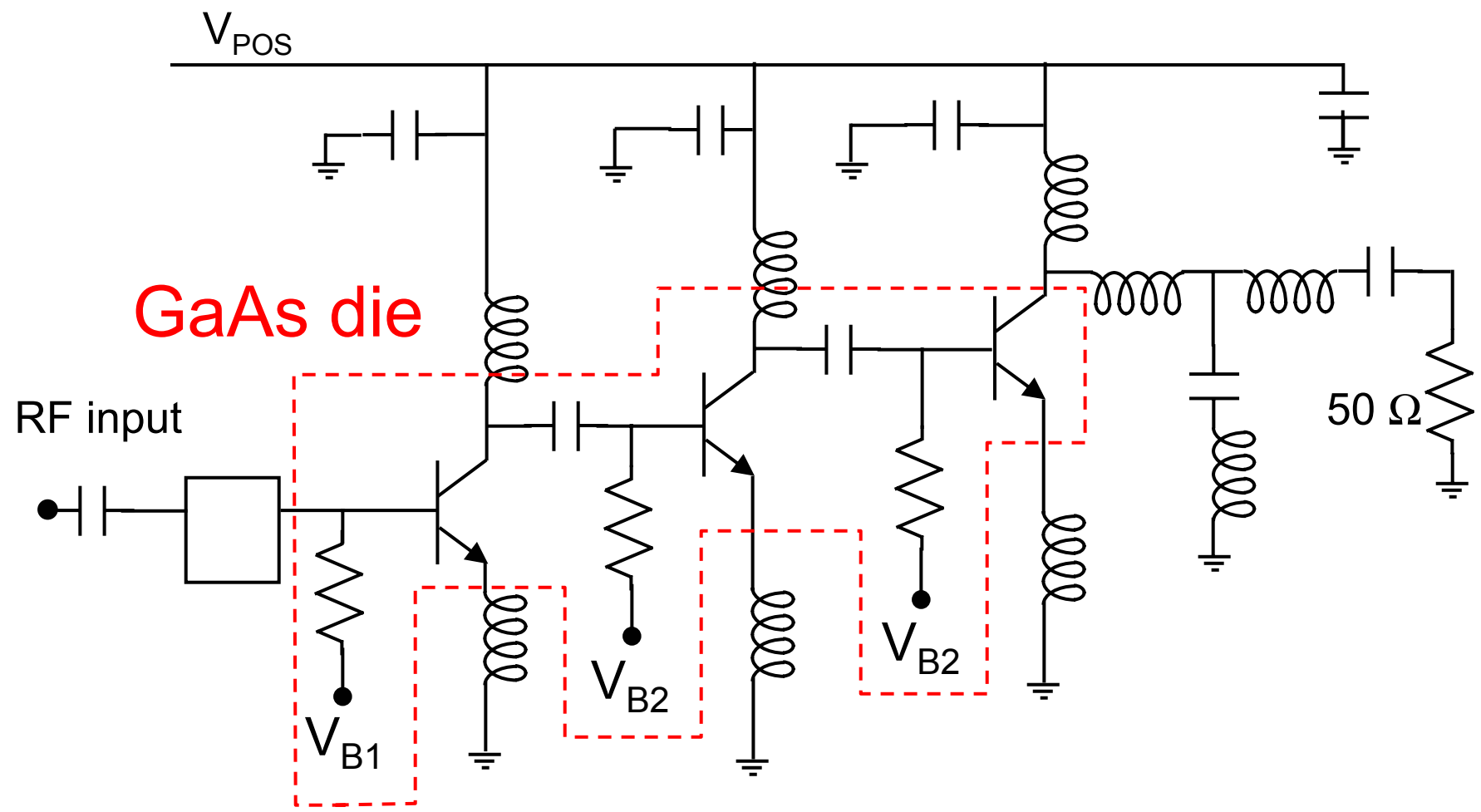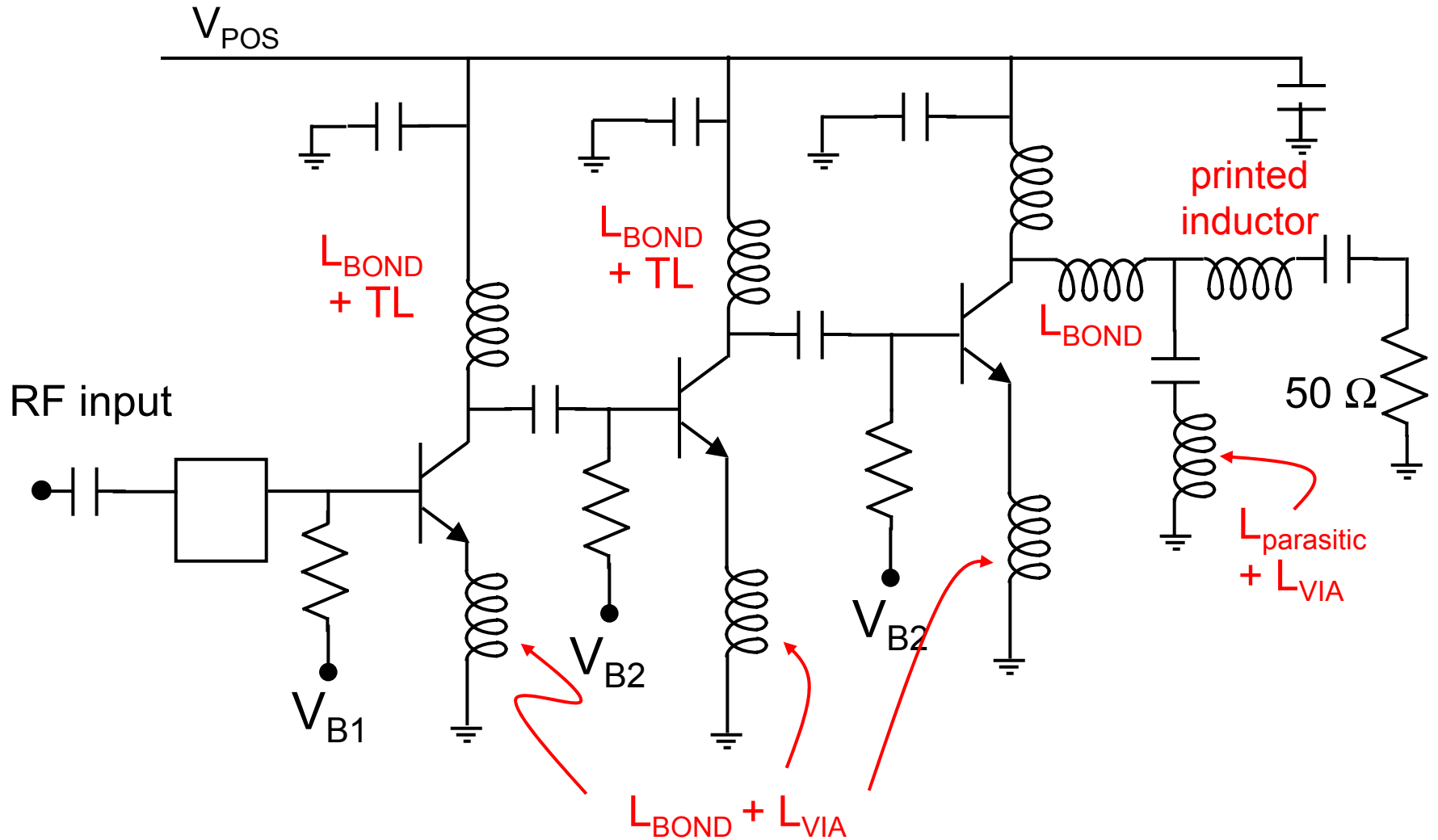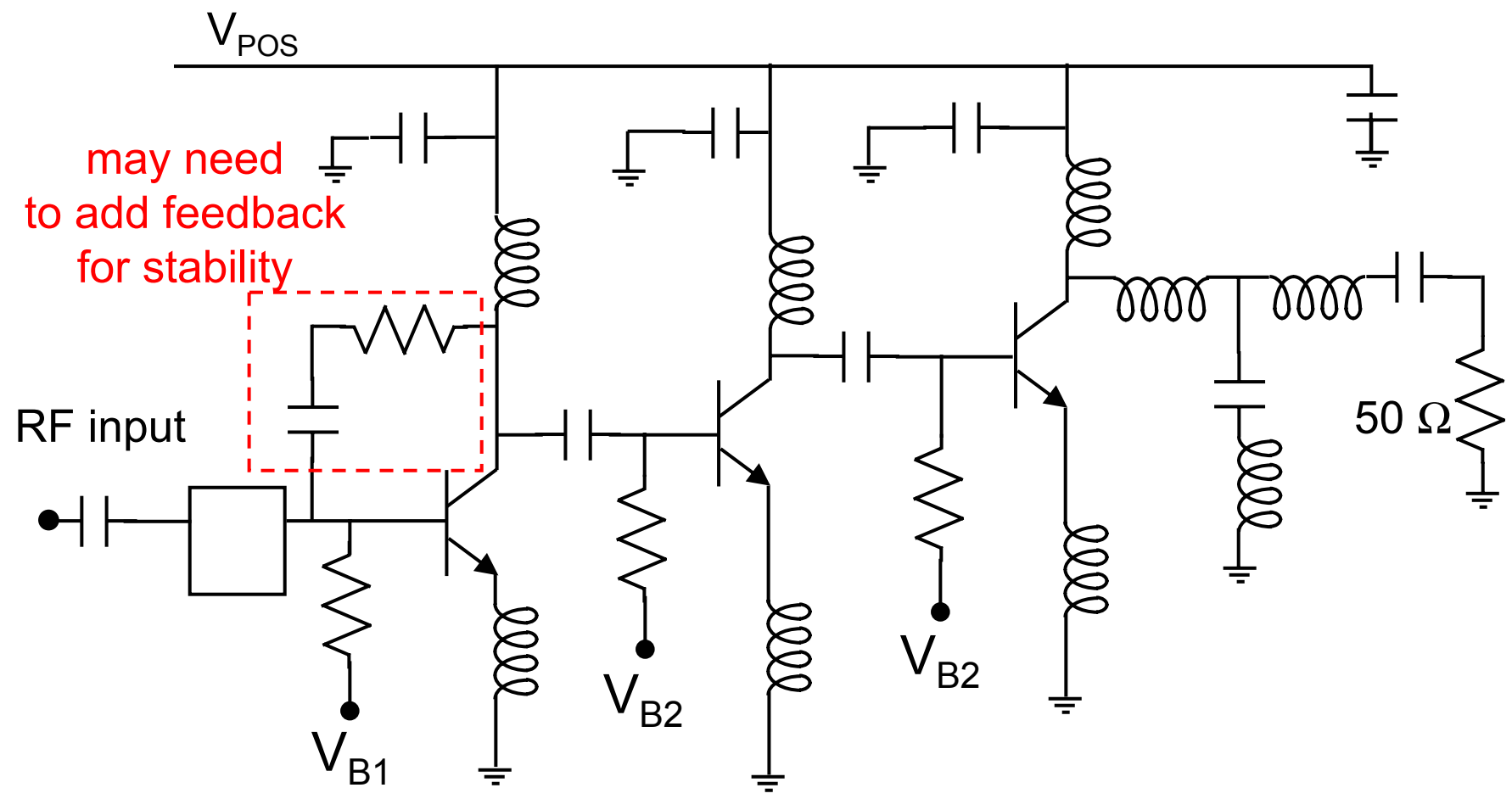
# Real-World Design Example: The Circuit

# Real-World Design Example: The Circuit



$V_{POS}$

Inter-stage match

RF input

$V_{B1}$

$V_{B2}$

$V_{B2}$

50 $\Omega$
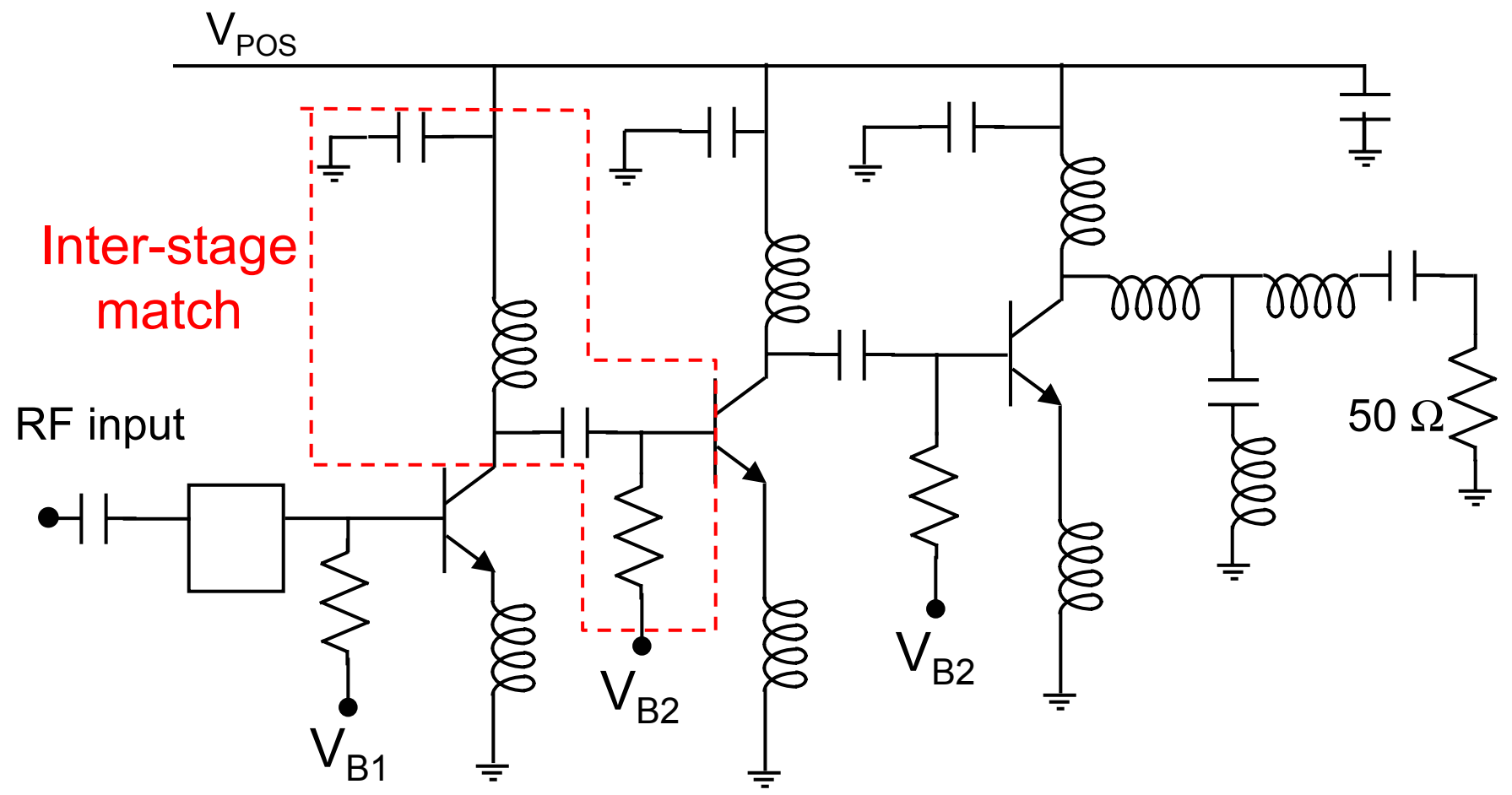
# Real-World Design Example

# Real-World Design Example



V_POS

may need
to add feedback
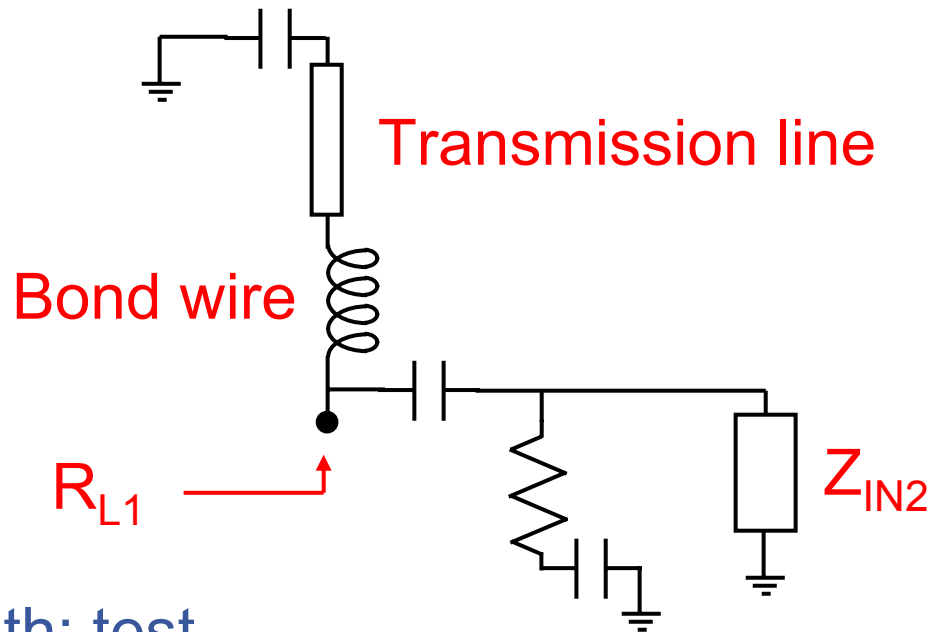for stability

RF input

50 Ω

V_B1

V_B2

V_B2

# Real-World Design Example: Tuning

◆ **Example of inter-stage match, 1st to 2nd stage**

$$R_{L1} = 194\ \Omega\ (?)$$
$$Z_{IN2} = 30 - j10\ (?)$$
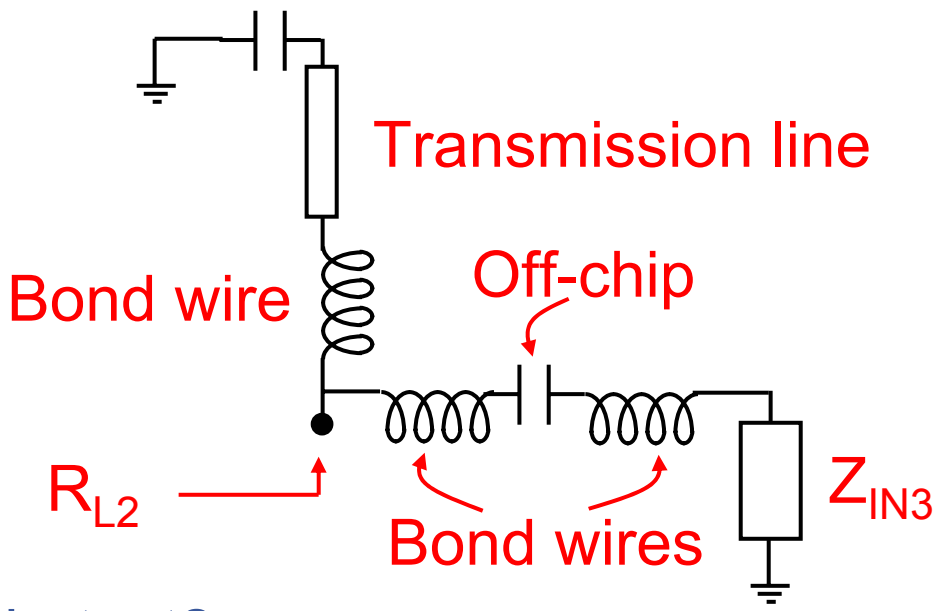
Both are really just guesses

Transmission line

Bond wire

$R_{L1}$

$Z_{IN2}$

\* Go to Winsmith: test

ANALOG
DEVICES

# Real-World Design Example: Tuning

◆ **Example of inter-stage match, 2$^{nd}$ to 3$^{rd}$ stage**
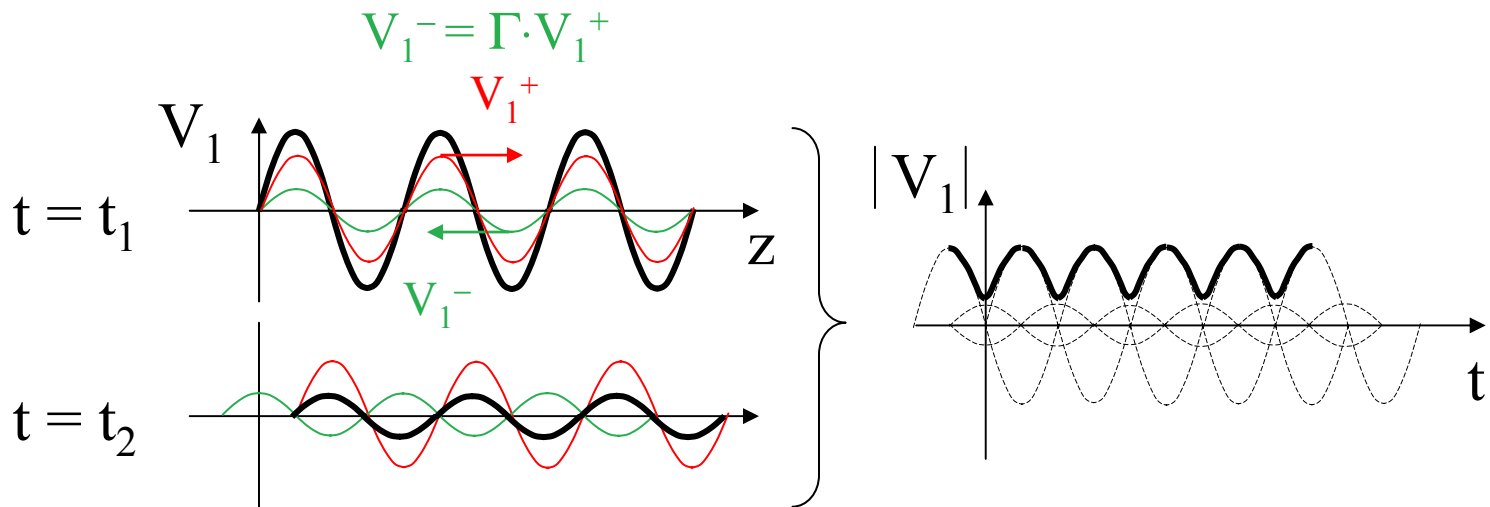
$$R_{L2} = 19.4 \ \Omega$$

$$Z_{IN3} = 2 - j2$$



Transmission line

Bond wire

Off-chip

$R_{L2}$

Bond wires

$Z_{IN3}$

\* Go to Winsmith: test2

ANALOG
DEVICES

# System Specifications

◆ **Ruggedness**

- **50 $\Omega$ load is for antenna in free space. Place antenna on a metal plate and can easily get VSWR of 4:1**

- **Typical PA specs are: don't oscillate at up to 4:1, survive up to 10:1 (!)**
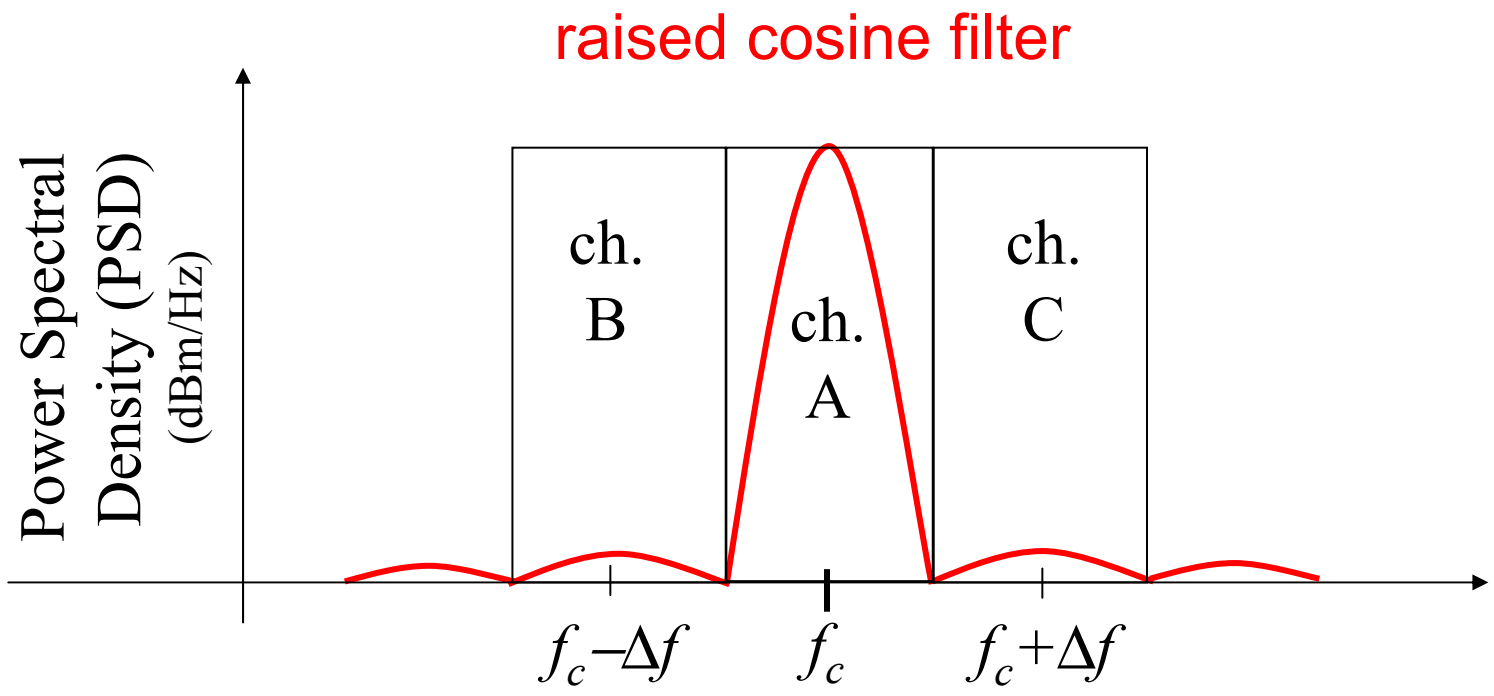


ANALOG
DEVICES

# System Specifications

◆ **Linearity**

- **For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important**

raised cosine filter



Power Spectral Density (PSD) (dBm/Hz)

ch. B

ch. A

ch. C

$f_c - \Delta f$　　$f_c$　　$f_c + \Delta f$

# System Specifications

- ◆ **Linearity**
  - ● **For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important**



3$^{rd}$ order distortion

Power Spectral Density (PSD) (dBm/Hz)

ch. B

ch. A

ch. C

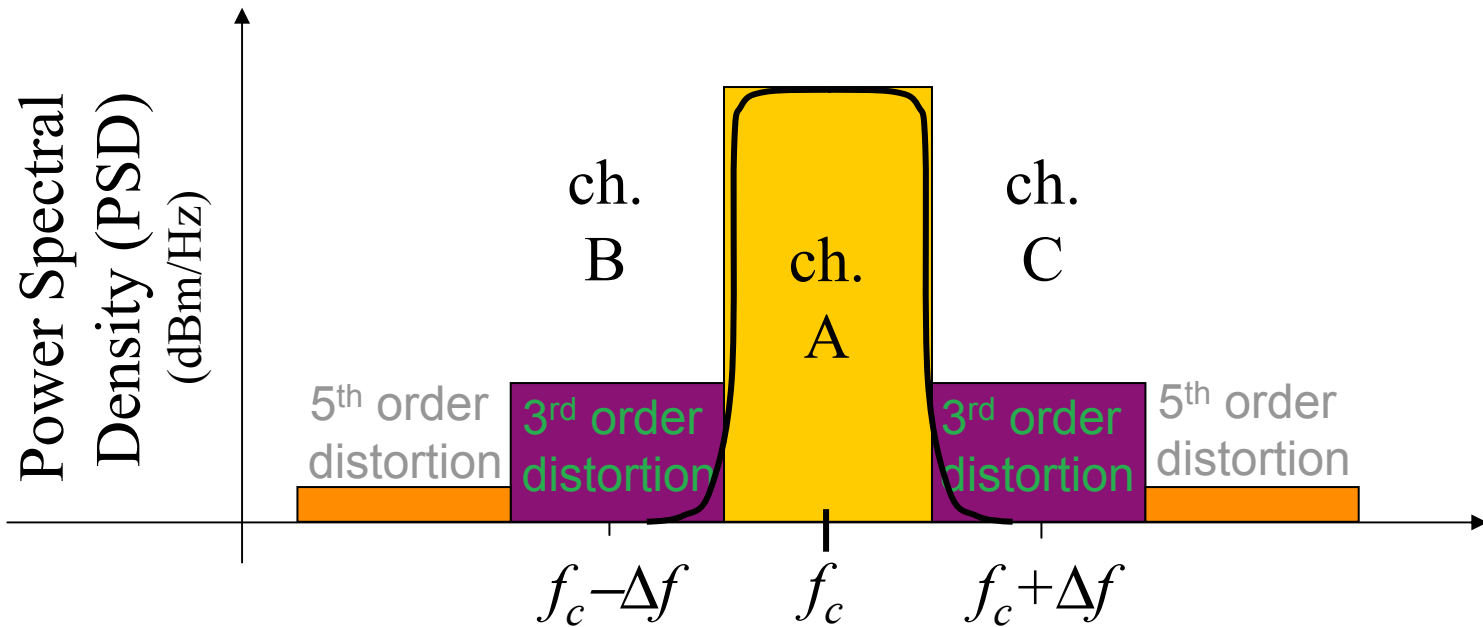$f_c - \Delta f$      $f_c$      $f_c + \Delta f$

# System Specifications

◆ **Linearity**

- **For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important**

# System Specifications

◆ **Linearity**

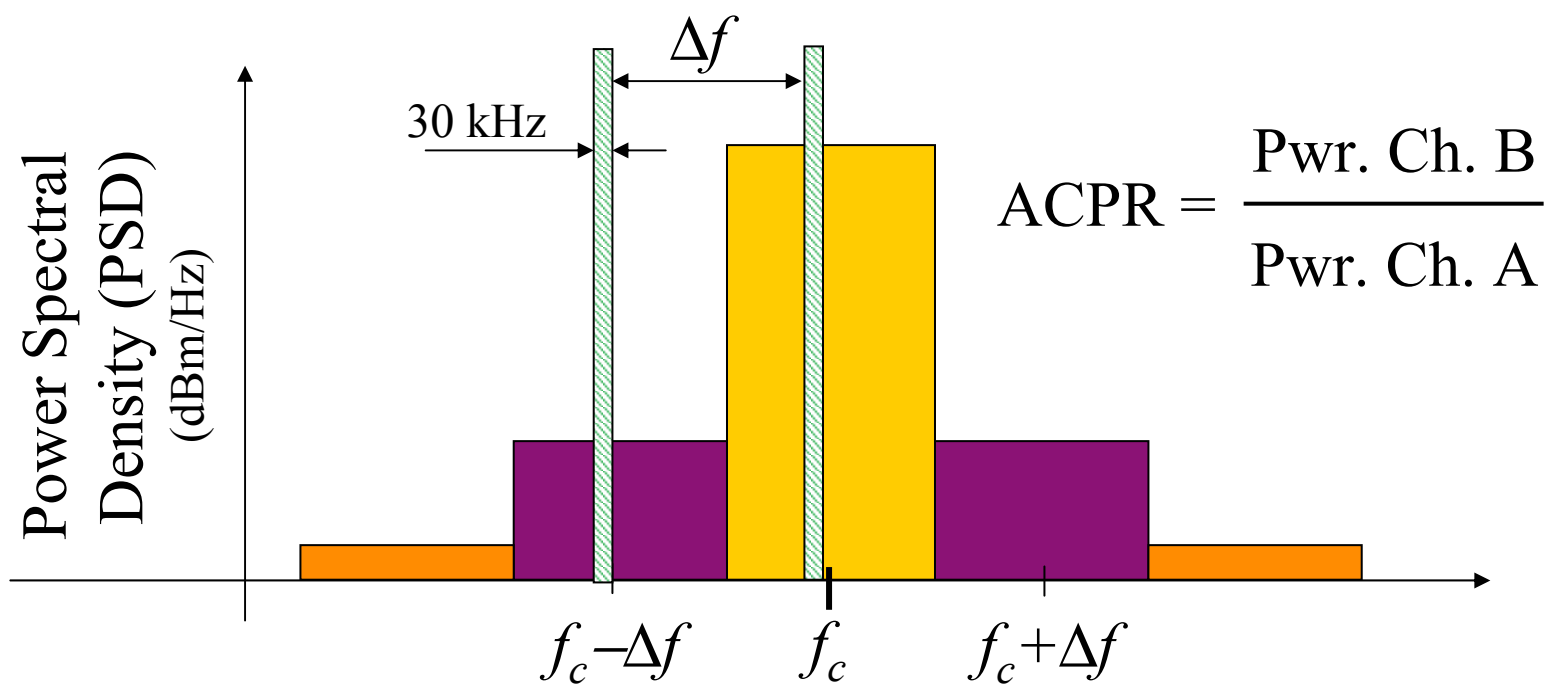● **For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important**



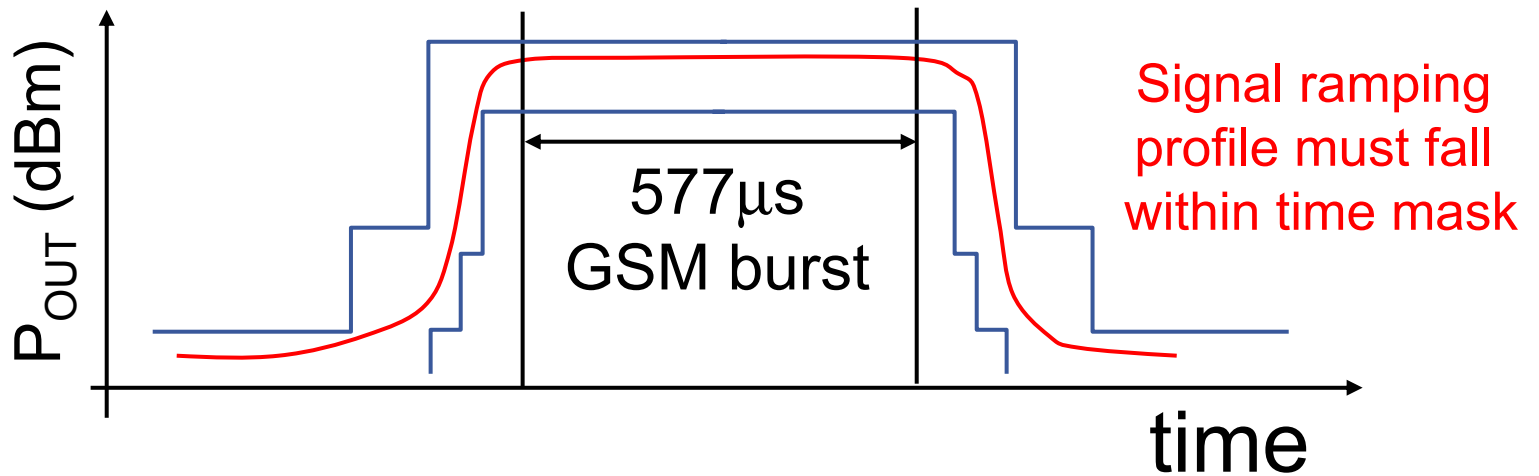$$\text{ACPR} = \frac{\text{Pwr. Ch. B}}{\text{Pwr. Ch. A}}$$

# System Specifications

- **Linearity**
  - **For non-linear PA in TDMA systems, harmonic spurs and switching transients are most common measure of linearity**
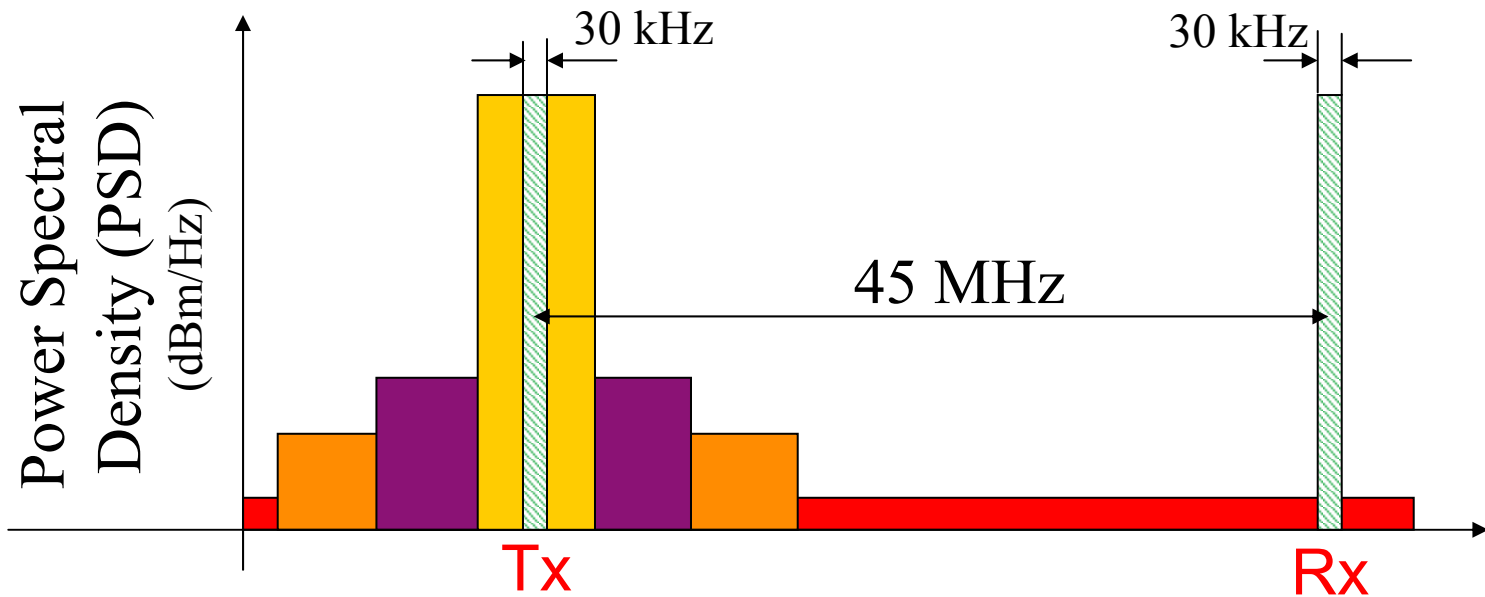


$P_{OUT}$ (dBm)

577µs
GSM burst

Signal ramping profile must fall within time mask

time

# System Specifications
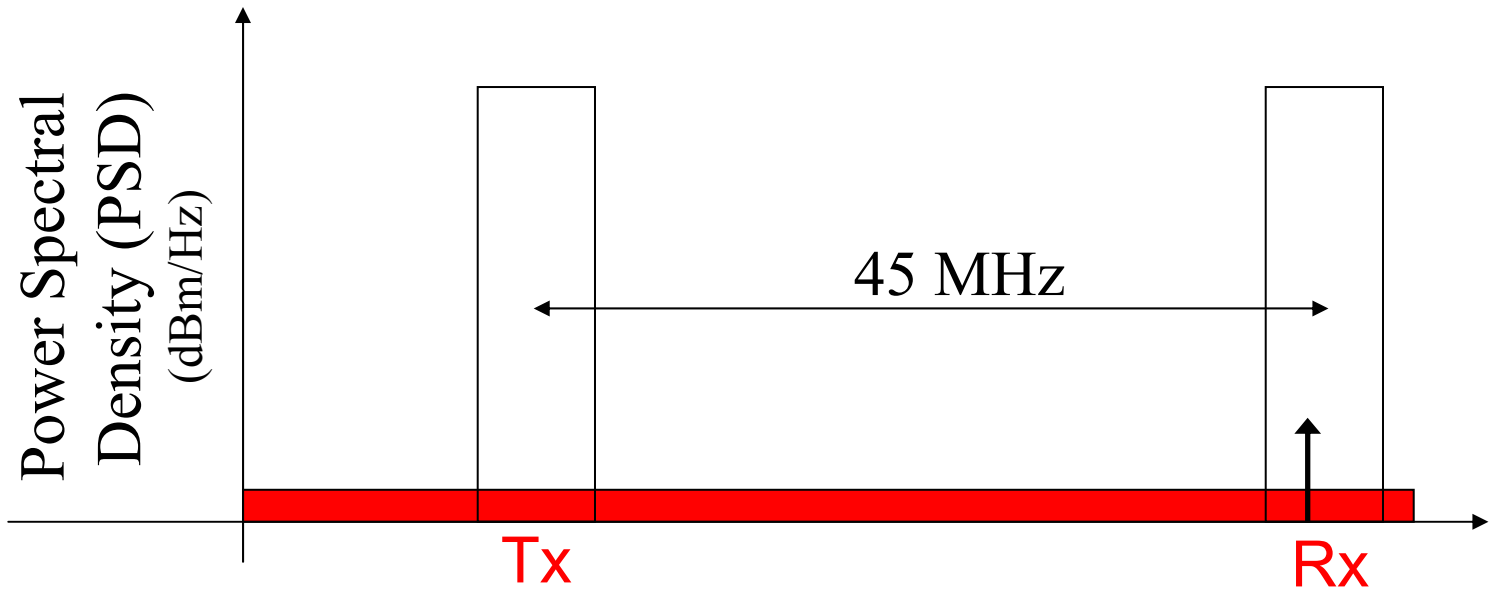
◆ **Noise in receive band:**

- **Obvious spec. in systems where Tx and Rx are operating at the same time (FDD)**

ANALOG
DEVICES

# System Specifications

◆ **Noise in receive band:**
- **Obvious spec. in systems where Tx and Rx are operating at the same time (FDD)**
- **Not so obvious spec in TDD system.  Problem primarily of mixing by the PA ($2\omega_2 - \omega_1$ or $\omega_2 - \omega_1$ )**

# Power Control

- **For linear PA, expected to operate at constant gain. Power control is therefore a function of $P_{IN}$.**
- **Role of bias circuitry is to maintain constant gain over $P_{IN}$, temperature (PTAT?).**



Power transistor
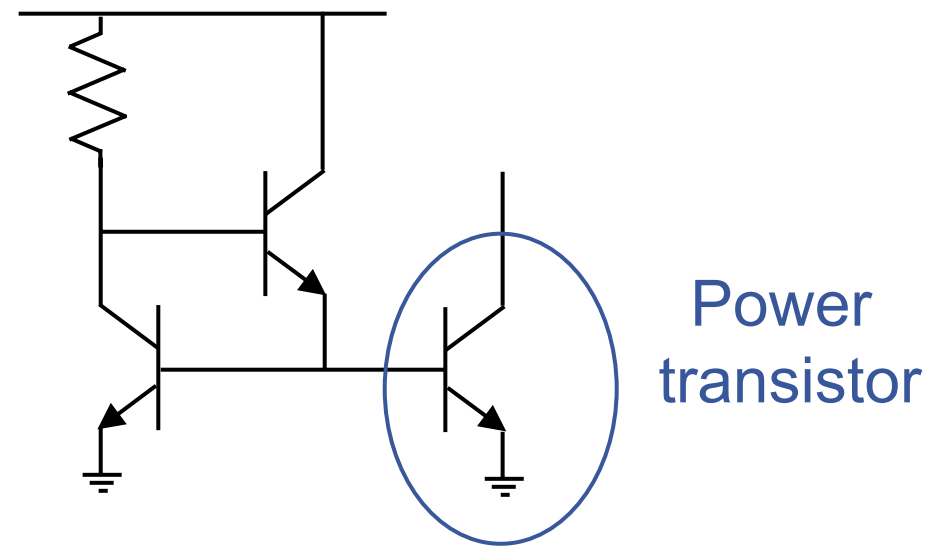
# Power Control

◆ **For non-linear PA, expected to operate at constant $P_{IN}$. Power control is achieved by varying gain.**

External control signal $V_{APC}$

On-chip bias circuitry

Power transistor